Features

- Fully Qualified Bluetooth v2.1 + EDR system
- Integrated FM Radio Receiver with RDS Demodulator
- Stereo Audio Output Stage
- Full-speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- Low-power 1.5V Operation, 1.8V to 3.6V I/O
- Integrated 1.8V and 1.5V Regulators
- USB v1.1 and UART with Dual Port Bypass Mode to 4Mbits/s
- UART Port to 4Mbits/s
- 0.4mm pitch WLCSP - no underfill required
- Support for 802.11 Coexistence
- RoHS Compliant

BlueCore™5-FM WLCSP

Single Chip Bluetooth® v2.1 + EDR System

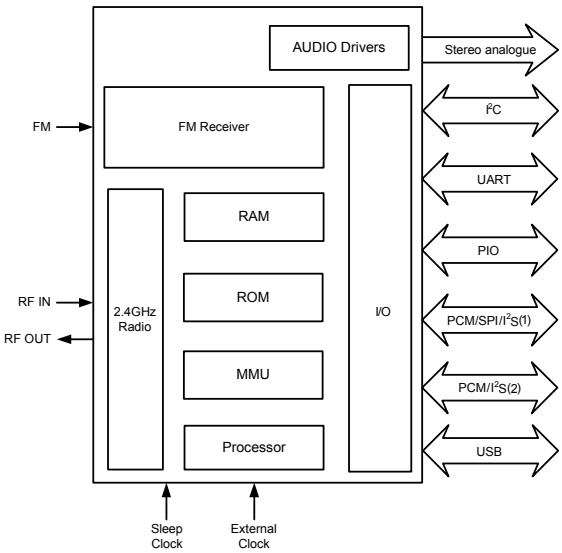
Advance Information Data Sheet for

September 2007

General Description

The **BlueCore™5-FM WLCSP** is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including enhanced data rates (EDR) to 3Mbits/s. It includes an integrated FM receiver with stereo audio output stage and an RDS demodulator.

With the on-chip CSR Bluetooth software stack, it provides a fully compliant Bluetooth system to v2.1 + EDR of the specification for data and voice communications.



System Architecture

Applications

- Cellular handsets
- Personal Digital Assistants (PDAs)

BlueCore5-FM WLCSP has been designed to reduce the number of external components required which ensures production costs are minimised.

The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.1 + EDR specification (all mandatory and optional features).

To improve the performance of both Bluetooth and 802.11b/g co-located systems a wide range of co-existence features are available including a variety of hardware signalling: basic activity signalling and Intel WCS activity and channel signalling.

BlueCore™5-FM WLCSP Product Data Sheet

Contents

List of Figures

List of Tables

List of Equations

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications and schematics may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-Critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

RoHS Compliance

BlueCore5-FM WLCSP devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

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While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

1 Device Details

Bluetooth Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- No external trimming is required in production
- Bluetooth v2.1 + EDR Specification compliant

Bluetooth Transmitter

- Class 2 transmit power with level control from on-chip 6-bit DAC over a dynamic range >20dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
-

Bluetooth Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Channel classification for AFH

Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter
- Compatible with external clock between 12 and 52MHz

FM Radio

- Simultaneous operation with Bluetooth
- Support of US/Europe (87.5 to 108MHz) and Japanese (76 to 90MHz) FM band
- Wide dynamic range AGC
- Soft mute and stereo blend
- Adjustment-free stereo decoder and AFC
- Autonomous search tuning function (up/down) with programmability (threshold setting)
- RDS demodulator
- Audio output available over Bluetooth audio interface or dedicated audio output
- Control of FM via Bluetooth HCI or I^2C
- Adaptive filter to suppress narrow band interference in the FM channel

Audio

- Single-ended stereo analogue output
- 16-bit 48kHz, digital audio bit stream output

Baseband and Software

- Internal 48kbyte RAM, allows full speed data transfer, mixed voice and data, and full piconet operation, including all medium rate packet types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Supports all Bluetooth v2.1 + EDR features incl. eSCO and AFH
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbits/s for system debugging
- UART interface with programmable baud rate up to 4Mbits/s with an optional bypass mode
- USB v1.1 interface
- I^2C slave for FM
- Two audio PCM interfaces (input and output)
- Analogue stereo (output only)

Auxiliary Features

- Power management includes digital shutdown, and wake-up commands with an integrated low-power oscillator for ultra-low power Park/Sniff/Hold mode
- Clock request output to control an external clock
- Device can run in low power modes from an external 32768Hz clock signal
- Auto Baud Rate setting, subject to host interface in use
- On-chip linear regulators: 1.8V output from typical 2.5-5.5V input to power I/O ring (load current 100mA) and second low dropout linear regulator producing 1.5V core voltage from 1.8V
- Power-on-reset cell detects low supply voltage
- Arbitrary sequencing of power supplies is permitted

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in the configuration:

- Standard HCI over UART

Package Options

- 67-ball 4.12 x 4.04 x 0.66mm, 0.4mm pitch WLCSP

2 Device Diagram

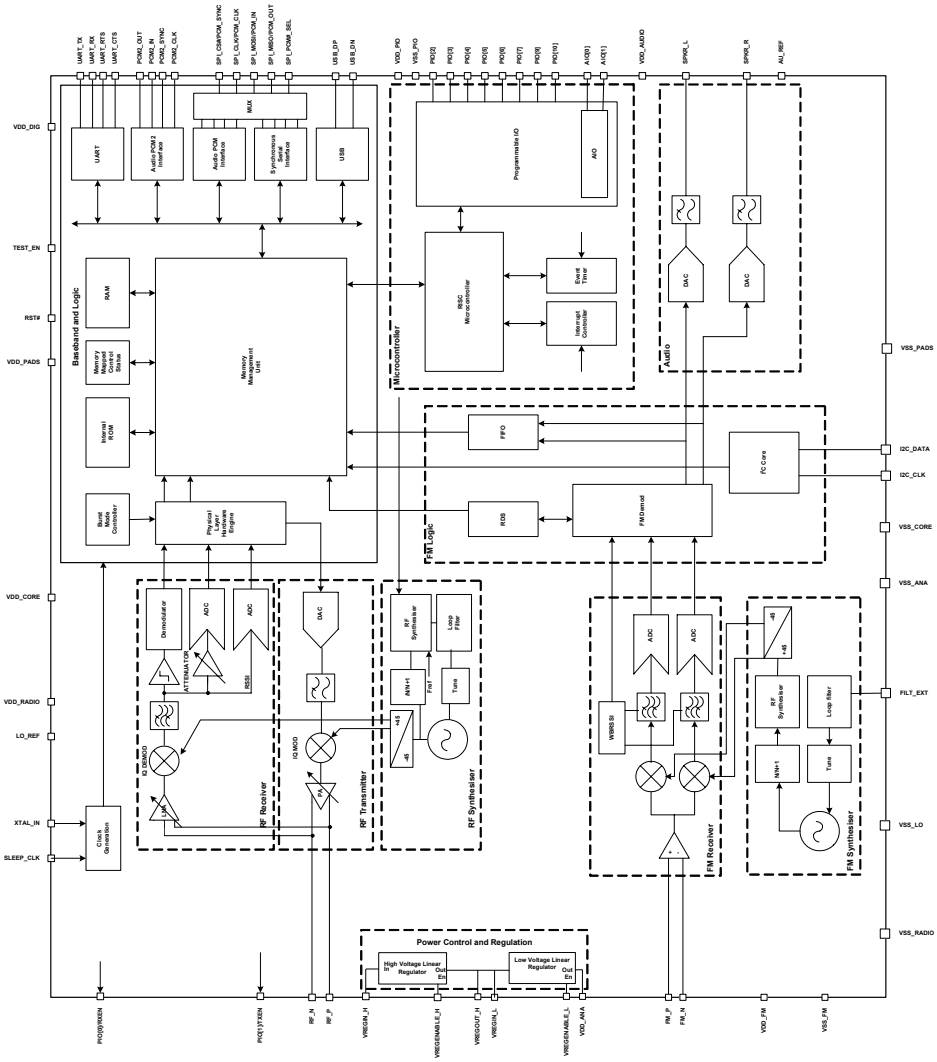


Figure 2.1: Device Diagram

3 Package Information

3.1 BlueCore5-FM WLCSP Package Information

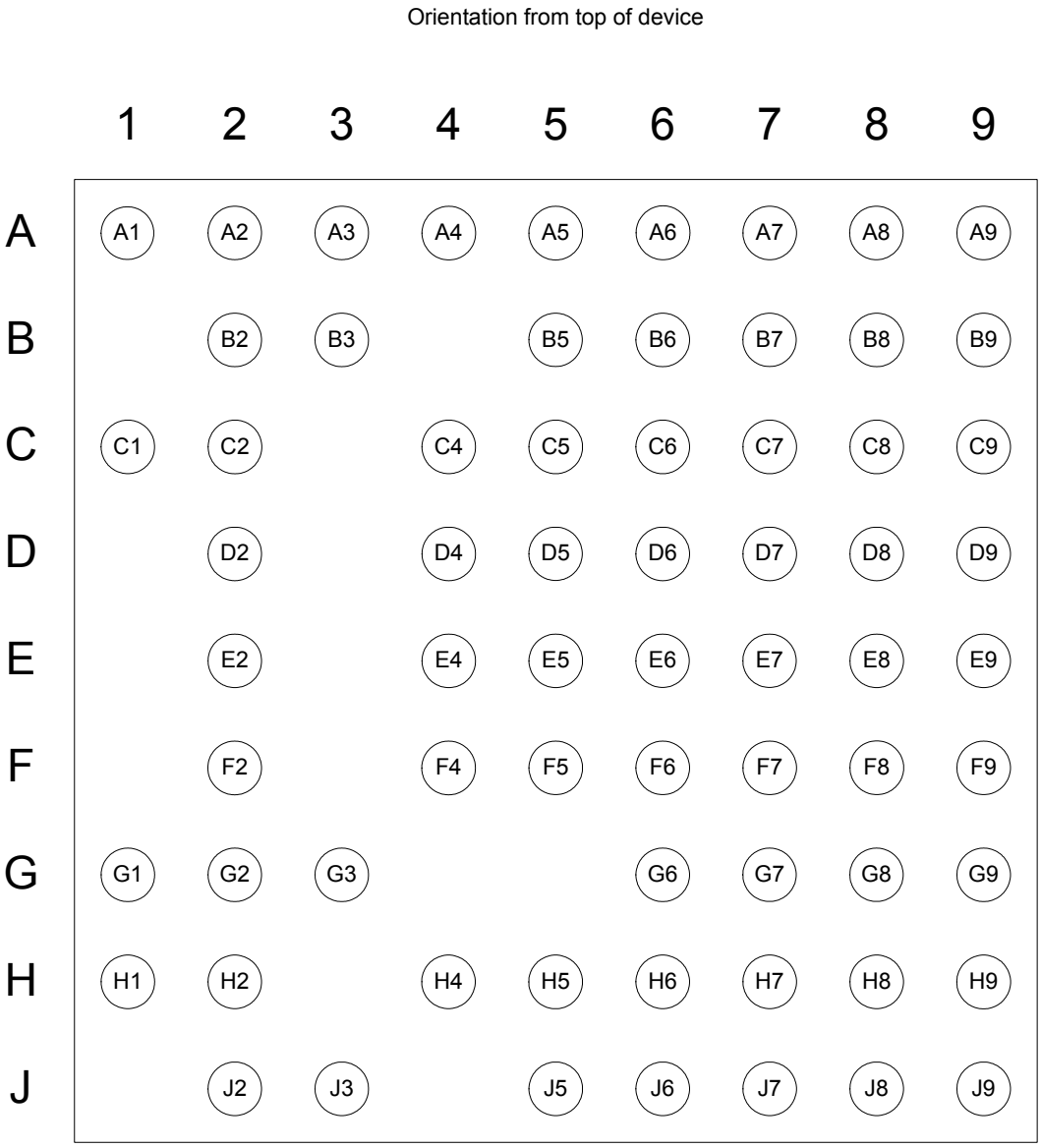


Figure 3.1: BlueCore5-FM WLCSP Device Pinout

3.2 Device Terminal Functions

Bluetooth Radio	Ball	Pad Type	Supply Domain	Description
RF_N	E2	RF	RADIO	Transmitter output/switched receiver input
RF_P	F2	RF	RADIO	Complement of RF_N

FM Radio	Ball	Pad Type	Supply Domain	Description
FM_N	H1	RF	FM	Receiver input
FM_P	G1	RF	FM	Complement of FM_N

Synthesiser and Oscillator	Ball	Pad Type	Supply Domain	Description
XTAL_IN	A3	Analogue	ANA	Reference clock input
SLEEP_CLK	G8	Input, with weak pull-down	PADS	32.768kHz clock input
LO_REF	A2	Analogue	ANA	Reference voltage decoupling
FILT_EXT	F4	Analogue	FM	External FM local oscillator loop filter

Audio	Ball	Pad Type	Supply Domain	Description
SPKR_L	H5	Analogue output	AUDIO	Analogue output, left
SPKR_R	J5	Analogue output	AUDIO	Analogue output, right
AU_REF	H4	Analogue	AUDIO	Audio reference voltage decoupling

PCM/SPI Interface (a)	Ball	Pad Type	Supply Domain	Description
PCM1_OUT	C8	Output, tri-state, with weak internal pull-down	PADS	Synchronous data output
SPI_MISO				SPI data output
PCM1_IN	C5	Input, with weak internal pull-down	PADS	Synchronous data input
SPI_MOSI				SPI data input
PCM1_SYNC	B9	Bi-directional with weak internal pull-down	PADS	Synchronous data sync
SPI_CS#				Chip select for Serial Peripheral Interface (SPI), active low
PCM1_CLK	D7	Bi-directional with weak internal pull-down	PADS	Synchronous data clock
SPI_CLK				SPI clock
SPI_PCM#_SEL	D6	Input with weak internal pull-down	PADS	Control line to select SPI or PCM interface: SPI_PCM#_SEL = 1 selects SPI SPI_PCM#_SEL = 0 selects PCM

(a) The PCM1 and SPI interfaces share the same pins. The interface is selected by SPI_PCM#_SEL.

PCM2 Interface	Ball	Pad Type	Supply Domain	Description
PCM2_OUT	F8	Output, tri-state, with weak internal pull-down	PADS	Synchronous data output
PCM2_IN	F9	Input, with weak internal pull-down	PADS	Synchronous data input
PCM2_SYNC	E4	Bi-directional with weak internal pull-down	PADS	Synchronous data sync
PCM2_CLK	F7	Bi-directional with weak internal pull-down	PADS	Synchronous data clock

UART and USB	Ball	Pad Type	Supply Domain	Description
UART_TX	A9	Bi-directional, tri-state, with weak internal pull-up	DIG	UART data output, active high
UART_RX	C7	Input with weak internal pull-down	DIG	UART data input, active high
UART_RTS	B7	Bi-directional input, with weak internal pull-up	DIG	UART request to send, active low
UART_CTS	A8	Input with weak internal pull-down	DIG	UART clear to send, active low
USB_DP	B6	Bi-directional	DIG	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	C6	Bi-directional	DIG	USB data minus

I^2C Interface (for FM control only)	Ball	Pad Type	Supply Domain	Description
I2C_CLK	G7	Input, with weak internal pull-up	PADS	I^2C clock
I2C_DATA	G9	Output, with weak internal pull-up	PADS	I^2C data

PIO Port	Ball	Pad Type	Supply Domain	Description
PIO[10]	J8	Bi-directional with programmable strength internal pull-up/down	PIO	Programmable input/output line
PIO[9]	F5	Bi-directional with programmable strength internal pull-up/down	PIO	Programmable input/output line
PIO[7]	E9	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line

PIO Port	Ball	Pad Type	Supply Domain	Description
PIO[6]	E7	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
PIO[5]	E6	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
PIO[4]	E5	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
PIO[3]	F6	Bi-directional with programmable strength internal pull-up/down	PIO	Programmable input/output line
PIO[2]	J9	Bi-directional with programmable strength internal pull-up/down	PIO	Programmable input/output line
PIO[1]	G6	Bi-directional with programmable strength internal pull-up/down	PIO	Programmable input/output line (external TXEN)
PIO[0]	H6	Bi-directional with programmable strength internal pull-up/down	PIO	Programmable input/output line (external RXEN)
AIO[1]	D4	Bi-directional	DIG	Analogue/digital programmable input/output line
AIO[0]	C4	Bi-directional	DIG	Analogue/digital programmable input/output line

Test and Debug	Ball	Pad Type	Supply Domain	Description
RST#	E8	Input with weak internal pull-up	PADS	Reset if low. Input debounced so must be low for >5ms to cause a reset
TEST_EN	D5	Input with strong internal pull-down	PADS	For test purposes only (leave unconnected)

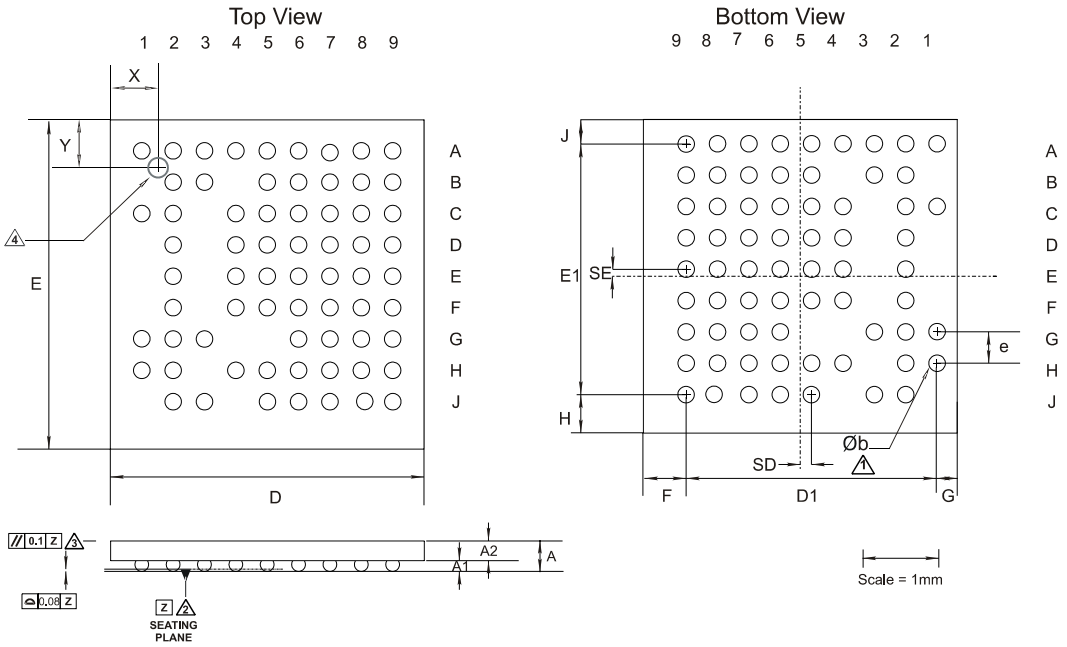
Power Supplies Control	Ball	Pad Type	Supply Domain	Description
VREGENABLE_L	A4	Input with weak internal pull-up	VREGENABLE_L	Take high to enable low-voltage regulator
VREGENABLE_H	B5	Input with weak internal pull-up	VREGENABLE_H	Take high to enable high-voltage regulator

Power Supplies	Ball	Pad Type	Description
VREGIN_L	B2	Analogue regulator input	Input to internal low-voltage regulator
VREGIN_H	A5	Analogue regulator input	Input to internal high-voltage regulator
VREGOUT_H	A6	Supply	High-voltage regulator output
VDD_PIO	H8	VDD	Positive supply for PIO [10:9] and [3:0]

Power Supplies	Ball	Pad Type	Description
VDD_DIG	A7	VDD	Positive supply for UART and USB
VDD_PADS	D9	VDD	Positive supply for all other digital input/output ports including PIO [7:4], high voltage regulator output
VDD_CORE	C9, J7	VDD	Positive supply for internal digital circuitry
VDD_FM	J3	VDD	Positive supply for FM circuitry
VDD_RADIO	H2	VDD	Positive supply for RF circuitry
VDD_AUDIO	J6	VDD	Positive supply for audio circuitry
VDD_ANA	A1	VDD	Positive supply for analogue circuitry, AIO[0], AIO[1]. Output from internal 1.5V regulator
VSS_PIO	H9	VSS	Ground connections for digital PIO circuitry
VSS_FM	J2	VSS	Ground connections for FM circuitry
VSS_RADIO	G2, G3	VSS	Ground connections for RF circuitry
VSS_ANA	B3	VSS	Ground connections for analogue circuitry
VSS_PADS	B8	VSS	Ground connections for digital I/O circuitry
VSS_CORE	D8, H7	VSS	Ground connections for internal digital circuitry
VSS_LO	C1	VSS	Ground connections for VCO and synthesiser

Ball	Description
C2, D2	No connection

3.3 Package Dimensions



Description	67-Ball Wafer-Level Chip Scale Package (WLCSP)			
Size	4.12 x 4.04 x 0.66mm (max.)			
Pitch	0.4mm			
Package Ball Land	240µm Ø			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A			0.66	(1) Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1		0.2		
A2		0.43		
b		0.25		(2) Datum Z is defined by the spherical crowns of the solder balls
D	4.02	4.12	4.22	
E	3.94	4.04	4.14	(3) Parallelism measurement shall exclude any effect of mark on top surface of package
e		0.4		
D1		3.2		
E1		3.2		(4) Topside-polarity mark. The dimensions of the polarity mark are 0.3mm diameter.
F	0.507	0.557	0.607	
G	0.313	0.363	0.413	
H	0.405	0.455	0.505	
J	0.335	0.385	0.435	
SD		0.097		
SE		0.035		
X		TBD		
Y		TBD		
JEDEC	Non JEDEC			
Unit	mm			

Figure 3.2: BlueCore5-FM WLCSP Package Dimensions

3.4 PCB Design and Assembly Considerations

3.4.1 4.12 x 4.04 x 0.66mm WLCSP 67-Ball Package

This section lists recommendations to achieve maximum board-level reliability of the 4.12 x 4.04 x 0.66mm WLCSP 67-Ball package:

- Non solder-mask defined (NSMD) lands (that is, lands smaller than the solder mask aperture) are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- Ideally, via-in-pad technology should be used to achieve truly NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred and this trace should be as thin as possible – taking into consideration its current carrying and the radio frequency (RF) requirements.
- 35µm thick (1oz) copper lands are recommended rather than 17µm thick (0.5oz). This results in a greater standoff which has been proven to provide greater reliability during thermal cycling.
- Land diameter should be 240µm +/-10µm to achieve optimum reliability.
- Solder paste is preferred to flux during the assembly process, because this adds to the final volume of solder in the joint, increasing its reliability.
- Where a nickel gold plating finish is used, the gold thickness should be kept below 0.5µ to prevent brittle gold/tin intermetallics forming in the solder.

3.4.2 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

4 Bluetooth RF Interface Description

4.1 Bluetooth Radio Ports

4.1.1 RF_N and RF_P

RF_N and RF_P form a complementary balanced pair. On transmit their outputs are combined using a balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally. Both terminals present similar complex impedances that require matching networks between them and the balun. Starting from the substrate (chip side), the outputs can each be modelled as an ideal current source in parallel with a lossy resistance and a capacitor. The package parasitics can be represented as an equivalent series inductance.

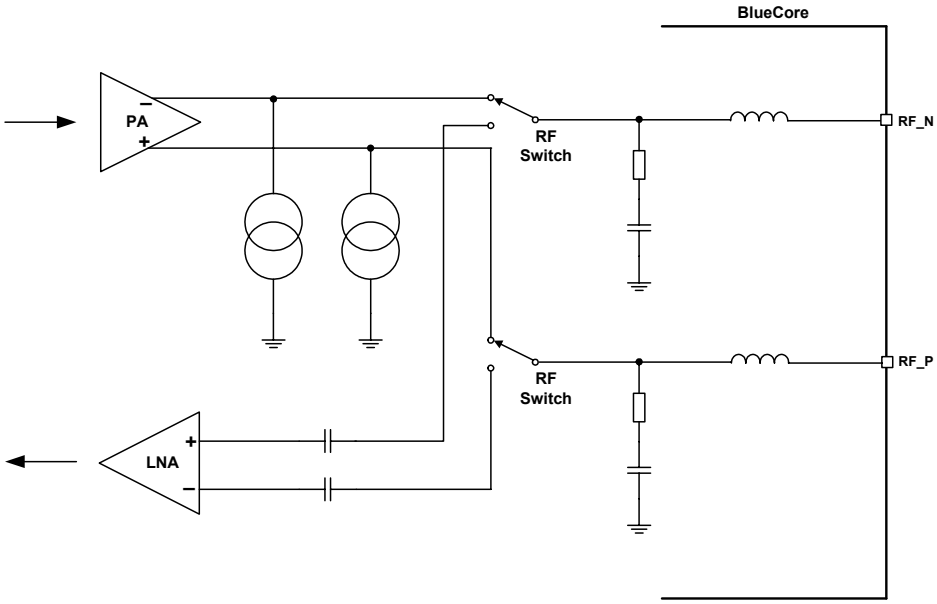


Figure 4.1: Simplified Circuit RF_N and RF_P

The DC level must be set at VDD_RADIO.

4.1.2 Control of External RF Components

TXRX_PIO_CONTROL (0x209) controls external RF components such as a switch, an external PA or an external LNA. PIO[0] and PIO[1] can be used for this purpose, as Table 4.1 shows.

TXRX_PIO_CONTROL Value	PIO Use
0	PIO[0] and PIO[1] not used to control RF. Power ramping is internal.
1	PIO[0] is high during RX, PIO[1] is high during TX. Power ramping is internal.
2	PIO[0] is high during RX, PIO[1] is high during TX. Power ramping is external.
3	PIO[0] is low during RX, PIO[1] is low during TX. Power ramping is external.
4	PIO[0] is high during RX, PIO[1] is high during TX. Power ramping is internal.

Table 4.1: TXRX_PIO_CONTROL Values

4.2 Bluetooth Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the receiver to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore5-FM WLCSP to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, an ADC digitises the IF received signal.

4.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the shared RF port.

4.2.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) implements fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

4.3 Bluetooth Transmitter

4.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

4.3.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm. This allows BlueCore5-FM WLCSP to be used in Class 2 and Class 3 Bluetooth radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

4.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

5 FM Radio

5.1 FM Receiver

The FM receiver fully supports reception over US/European (87.5MHz to 108MHz) and Japanese (76MHz to 90MHz) FM bands. The FM receiver comprises an RF receiver with fully integrated VCO, a stereo FM demodulator and an RDS demodulator.

The FM and RDS demodulators are implemented using digital processing. This provides excellent sensitivity, selectivity and audio quality. All the trims required by the FM demodulator are automatic, and its relevant parameters are programmable.

The FM receiver incorporates signal strength-dependent stereo blend and soft mute to preserve audio quality in fading conditions.

The FM receiver also includes special proprietary processing to reject interference. This allows for good quality reception of FM channels that would otherwise be corrupted due to pick-up of interference.

5.2 FM Digital Demodulator

The FM demodulation and the stereo multiplex processing are performed using digital hardware. A received signal strength indicator allows mono/stereo blending according to the quality of the signal. The RDS signal is demodulated and the RDS bit stream is supplied for processing in software. Figure 5.1 shows an outline of the FM digital hardware.

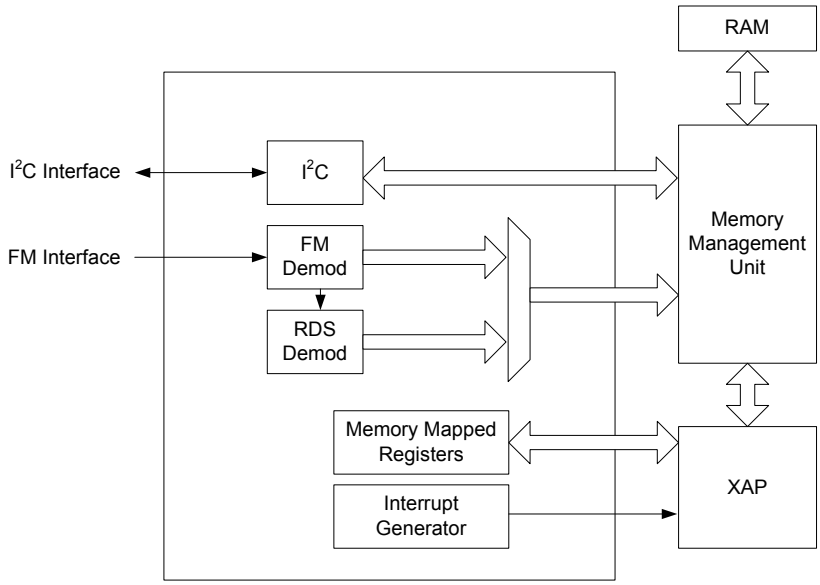


Figure 5.1: FM Demodulator Digital Hardware

The digital samples from the FM block are stored in a ring buffer in the shared RAM. The FM audio data is sourced from this buffer to either the stereo codec or the I²S interface or both. In addition to the FM audio data, the RDS data samples are also stored in RAM. When the amount of stored RDS data passes a programmed threshold, the host is interrupted.

5.3 Waking up the FM System

The FM subsystem is woken from deep sleep by issuing a command over the I²C interface. Refer to *BlueCore5-FM FM API* for more information. An interrupt is issued from the I²C module when a command with a valid address is received over the interface. This interrupt causes BlueCore5-FM to exit from deep sleep mode and allows the I²C interface to transfer the received bytes to RAM via the memory management unit. The firmware can then act appropriately on the command, enabling the FM subsystem if required and requesting the reference clock from the host if required.

5.4 FM Search Tuning

Table 5.1 shows the times for the FM search tuning operation to scan all channels in a band. These are the times for a scan of the complete band when all stations in the band have a received power level below the search threshold..

FM Band	Channel Spacing	Search Tuning Time	
		Typ	Max
87.7-108Mhz	100kHz	1.0s	1.1s
76-90MHz	100kHz	0.7s	0.8s

Table 5.1: FM Search Tuning Time

NoteChanging the tone rejection settings in PSKEY_FM_TONEREJ_FREQS may increase the search tuning time.

5.5 BCCMD/HQ

Commands initiated by the host are conveyed with a BCCMD. This is used for both register reads and writes.

The format of BCCMD is defined in the CSR publication *BCCMD Commands* (CS-101482-SPP (bcore-sp-005P)).

Events are signalled to the host by the generation of an HQ message. These events may be masked.

The format of HQ is defined in the CSR publication *HQ Commands* (CS-101677-SPP (bcore-sp-003P)).

5.6 FM API and Configuration

For information refer to *BlueCore5-FM FM API*.

6 Clock Generation

6.1 Clock Input and Generation

The Bluetooth reference clock for the system is generated from an external clock source of between 12MHz and 52MHz.

All BlueCore5-FM WLCSP internal digital clocks are generated using a phase locked loop, which is locked to the frequency of either the external 12MHz to 52MHz reference clock source, or a Sleep Clock frequency of 32.768kHz.

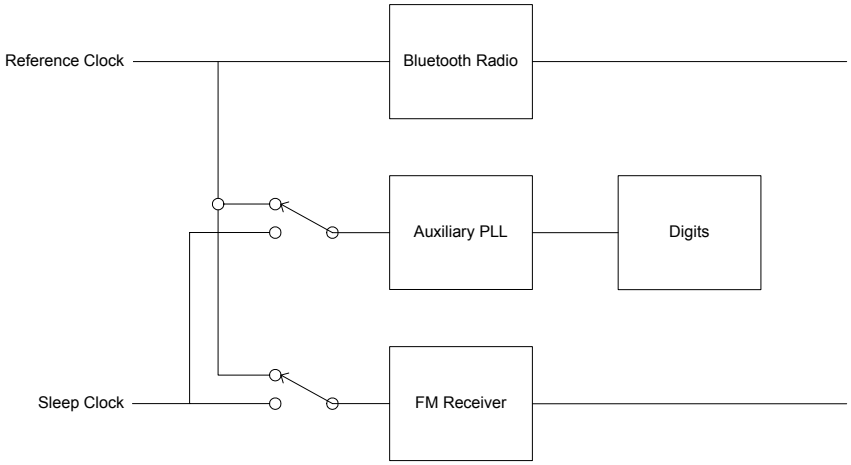


Figure 6.1: Clock Architecture

The Auxiliary PLL may use either clock source. The clock presented to the internal digital logic is the same in both cases. The use of the Sleep Clock is to be determined with respect to Bluetooth and FM operation in low power modes.

6.1.1 Input Frequencies and PS Key Settings

BlueCore5-FM WLCSP must be configured to operate with the chosen reference frequency. This is accomplished by setting PSKEY_ANA_FREQ (0x01FE) for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore5-FM WLCSP is 26MHz, depending on the firmware build. The minimum is 12MHz and the maximum is 52MHz. Full details are in the software release note for your specific firmware build on *www.csrsupport.com*.

The following CDMA/3G TCXO frequencies are also catered for: 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz. The value of the PS Key is a multiple of 1kHz. Hence 38.4MHz is selected by using a PS Key value of 38400.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (0x1fe) (Units of 1kHz)
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 250kHz	-
+26.00 Default	26000

Table 6.1: PS Key Values for CDMA/3G Phone TCXO

6.1.2 External Reference Clock

Input (XTAL_IN)

The external reference clock is applied to the BlueCore5-FM WLCSP XTAL_IN input.

The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion. If peaks of the reference clock are either below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (approximately 33pF) connected to XTAL_IN.

The external reference clock signal should meet the specifications outlined in Table 6.2.

			Min	Typ	Max
Frequency[a]			12MHz	26MHz	52MHz
Frequency tolerance			-20ppm	-	+20ppm
Duty cycle			20:80	50:50	80:20
Edge jitter (at zero crossing)			-	-	15ps rms
Signal level	AC coupled sinusoidal		400mV pk-pk	-	VDD_ANA[b]
	DC coupled digital	V_{IL}	-	VSS_ANA[c]	-
		V_{IH}	-	VDD_ANA[b][c]	-

Table 6.2: External Clock Specifications

(a) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

(b) VDD_ANA is 1.5V nominal

(c) If driven via a DC blocking capacitor max amplitude is reduced to 750mV pk-pk for non 50:50 duty cycle

XTAL_IN Impedance in External Mode

The impedance of XTAL_IN does not change significantly between operating modes, typically 10fF. When transitioning from Deep Sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input be used.

Clock Start-up Delay

BlueCore5-FM WLCSP hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore5-FM WLCSP firmware provides a software function that extends the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 1-31ms. Zero is the default for 5ms delay.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore5-FM WLCSP as low as possible. BlueCore5-FM WLCSP consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

6.1.3 Clock Timing Accuracy

As Figure 6.2 indicates, the 250ppm timing accuracy on the external clock is required 2ms after the firmware begins to run. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.1 + EDR Specification. Radio activity may occur after 6ms after the firmware starts. Therefore, at this point the timing accuracy of the external clock source must be within ±20ppm.

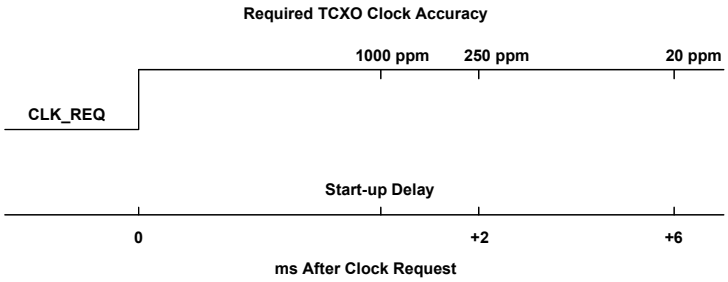


Figure 6.2: TCXO Clock Accuracy

7 Microcontroller, Memory and Baseband Logic

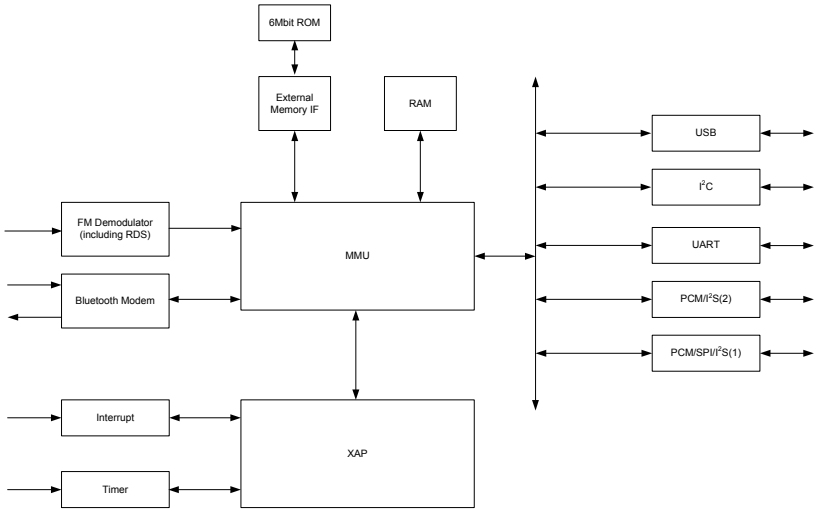


Figure 7.1: Baseband Digits Block Diagram

7.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.2 Burst Mode Controller

During transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

7.3 Physical Layer Hardware Engine DSP

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all optional and mandatory features of Bluetooth v2.1 + EDR including AFH and eSCO.

7.4 System RAM

48KB of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

7.5 ROM

6Mbits of metal programmable ROM is provided for system firmware implementation.

7.6 Microcontroller

The microcontroller (MCU), also known as XAP, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

7.7 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore5-FM WLCSP where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore5-FM WLCSP.

Note:

To turn on the clock, the clock enable signal on PIO[3] must be high.

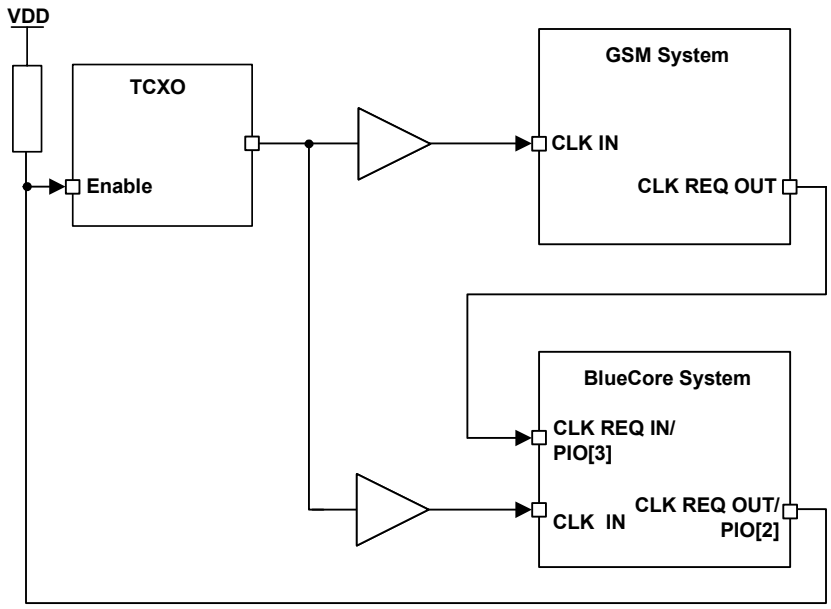


Figure 7.2: Example TCXO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] is tri-state. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

7.8 WLAN Co-Existence Interface

Dedicated hardware is provided to implement a variety of co-existence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware.

For more information see *Bluetooth and IEEE 802.11 b/g Co-existence Solutions Overview*.

7.9 Configurable I/O Parallel Ports

12 lines of programmable bi-directional input/outputs (I/O) are provided. PIO[10:9] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO[1:0] are powered from VDD_ANA.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset and have additional individual bus keeper configuration.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO[2] can be configured as a request line for an external clock source. Using PSKEY_CLOCK_REQUEST_ENABLE (0x246), this terminal can be configured to be low when BlueCore5-FM WLCSP is in Deep Sleep and high when a clock is required. See also section 7.7.

CSR cannot guarantee that the PIO assignments remain as described. Refer to the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

BlueCore5-FM WLCSP has two general-purpose analogue interface pins, AIO[0] and AIO[1]. These are used to access internal circuitry and control signals. Auxiliary functions available via these pins include a 10-bit ADC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals: 64, 48, 32, 16, 12MHz and the XTAL clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage. When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_ANA.

7.9.1 FM Receiver Interrupt

The BlueCore5-FM WLCSP default configuration assigns the FM_IRQ signal to PIO[10].

8 Serial Interfaces

8.1 UART Interface

This is a standard UART interface for communicating with other serial devices.

BlueCore5-FM WLCSP UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.(1)

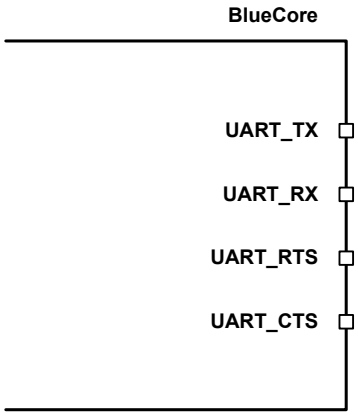


Figure 8.1: Universal Asynchronous Receiver

Four signals implement the UART function, as shown in Figure 8.1. When BlueCore5-FM WLCSP is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore5-FM WLCSP firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

Table 8.1: Possible UART Settings

The UART interface is capable of resetting BlueCore5-FM WLCSP on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 8.2. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOSTIO_UART_RESET_TIMEOUT, (0x1a4), a reset occurs. This feature allows a host to initialise the system to a known state. Also, BlueCore5-FM WLCSP can emit a break character that may be used to wake the host.

(1) Uses RS232 protocol, but voltage levels are 0V to VDD_DIG(requires external RS232 transceiver chip).

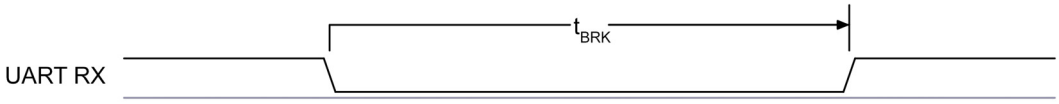


Figure 8.2: Break Signal

Table 8.2 shows a list of commonly used baud rates and their associated values for the PS Key PSKEY_UART_BAUDRATE (0x1be). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 8.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 8.1: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%

Table 8.2: Standard Baud Rates

8.1.1 UART Bypass

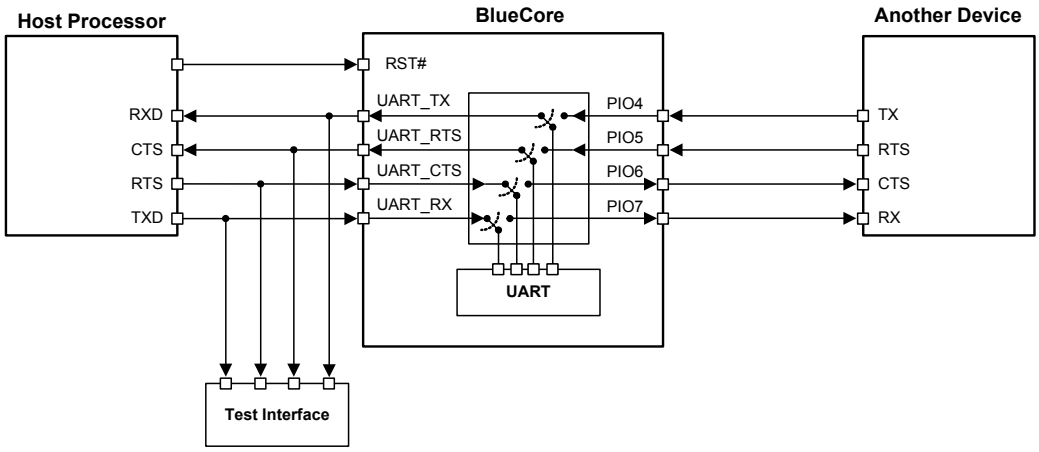


Figure 8.3: UART Bypass Architecture

8.1.2 UART Configuration While Reset is Active

The UART interface for BlueCore5-FM WLCSP is tri-state while the chip is being held in reset. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore5-FM WLCSP reset is de-asserted and the firmware begins to run.

8.1.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore5-FM WLCSP can be used. The default state of BlueCore5-FM WLCSP after reset is de-asserted; this is for the host UART bus to be connected to the BlueCore5-FM WLCSP UART, thereby allowing communication to BlueCore5-FM WLCSP via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.(1)

To apply the UART bypass mode, a BCCMD command is issued to BlueCore5-FM WLCSP. Upon this issue, it switches the bypass to PIO[7:4] as Figure 8.3 shows. When the bypass mode has been invoked, BlueCore5-FM WLCSP enters the Deep Sleep state indefinitely.

To re-establish communication with BlueCore5-FM WLCSP, the chip must be reset so that the default configuration takes effect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore, it is not possible to have active Bluetooth links while operating the bypass mode.

8.1.4 Current Consumption in UART Bypass Mode

The current consumption for a device in UART bypass mode is equal to the values quoted for a device in standby mode.

8.2 USB Interface

This is a full speed (12Mbits/s) Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore5-FM WLCSP acts as a USB peripheral, responding to requests from a master host controller such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.1+EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

(1) The range of the signalling level for the standard UART described in section 8.1 and the UART bypass may differ between CSR's BlueCore devices, as the power supply configurations are chip dependent. For BlueCore5-FM WLCSP, the standard UART is supplied by VDD_DIG, so has signalling levels of 0V and VDD_DIG. Whereas in the UART bypass mode, the signals appear on PIO[4:7] which are supplied by VDD_PADS, therefore the signalling levels are 0V and VDD_PADS.

As USB is a master/slave oriented system (in common with other USB peripherals), BlueCore5-FM WLCSP only supports USB Slave operation.

8.2.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore5-FM WLCSP, therefore, have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP/USB_DN and the cable.

8.2.2 USB Pull-Up Resistor

BlueCore5-FM WLCSP features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore5-FM WLCSP is ready to enumerate. It signals to the PC that it is a full speed (12Mbits/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD_PADS=3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

8.2.3 USB Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_DIG supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

8.2.4 Self-Powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore5-FM WLCSP via a resistor network (R_{vb1} and R_{vb2}), so BlueCore5-FM WLCSP can detect when VBUS is powered up. BlueCore5-FM WLCSP will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5kΩ ±5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in BlueCore is only suitable for bus-powered USB devices, e.g., dongles.

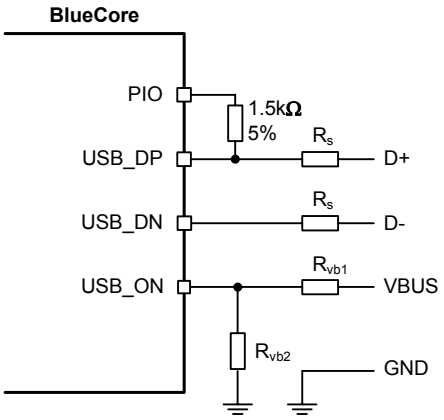


Figure 8.4: USB Connections for Self-Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

Note:

USB_ON is shared with BlueCore5-FM WLCSP PIO terminals.

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	22kΩ ±5%	VBUS ON sense divider
R_{vb2}	47kΩ ±5%	VBUS ON sense divider

Table 8.3: USB Interface Component Values

8.2.5 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore5-FM WLCSP negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, BlueCore5-FM WLCSP requests 100mA during enumeration.

For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting the PS Key PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See USB Specification v1.1, section 7.2.4.1. Some applications may require soft start circuitry to limit inrush current if more than 10μF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore5-FM WLCSP will result in reduced receive sensitivity and a distorted RF transmit signal.

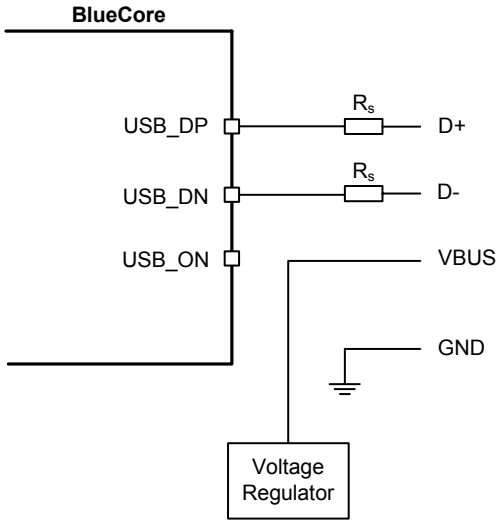


Figure 8.5: USB Connections for Bus-Powered Mode

8.2.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB suspend mode. While in USB Suspend, bus-powered devices must not draw more than 0.5mA from USB VBUS (self-powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus-powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100μA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore5-FM WLCSP. The entire circuit must be able to enter the suspend mode. Refer to separate CSR documentation for more details on USB Suspend.

8.2.7 Detach and Wake_Up Signalling

BlueCore5-FM WLCSP can provide out-of-band signalling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore5-FM WLCSP into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore5-FM WLCSP to put USB_DN and USB_DP in a high impedance state and turns off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore5-FM WLCSP will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable) and cannot be sent while BlueCore5-FM WLCSP is effectively disconnected from the bus.

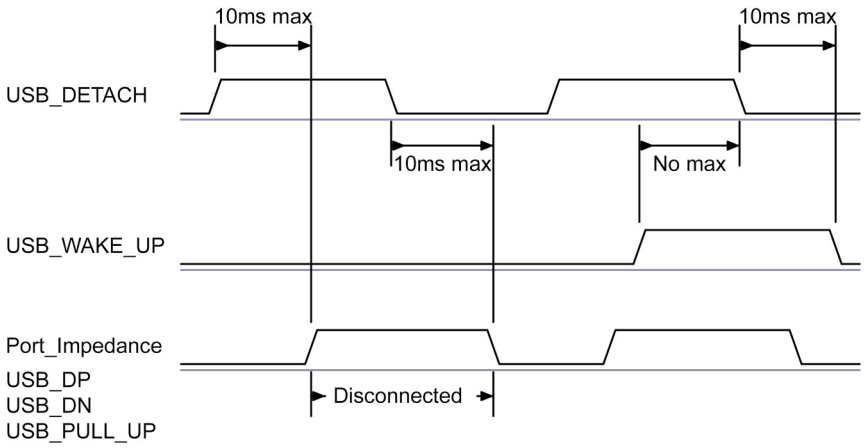


Figure 8.6: USB_DETACH and USB_WAKE_UP Signal

8.2.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore5-FM WLCSP and the Bluetooth software running on the host computer. Suitable drivers are available from http://www.csrsupport.com.

8.2.9 USB 1.1 Compliance

BlueCore5-FM WLCSP is qualified to the USB Specification v1.1, details of which are available from www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore5-FM WLCSP meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification v2.0 (Chapter 7) electrical requirements.

8.2.10 USB 2.0 Compatibility

BlueCore5-FM WLCSP is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

8.3 Serial Peripheral Interface

BlueCore5-FM WLCSP uses a 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore5-FM WLCSP via the SPI. The SPI and PCM interface share the same physical set of pins, selected using SPI_PCM#_SEL:

- SPI_PCM#_SEL = 1 selects SPI
- SPI_PCM#_SEL = 0 selects PCM

Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

8.3.1 Instruction Cycle

The BlueCore5-FM WLCSP is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 8.4 shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Table 8.4: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore5-FM WLCSP on the rising edge of the clock line SPI_CLK. When reading, BlueCore5-FM WLCSP replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore5-FM WLCSP offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

8.3.2 Writing to the Device

To write to BlueCore5-FM WLCSP, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CS# is taken high.

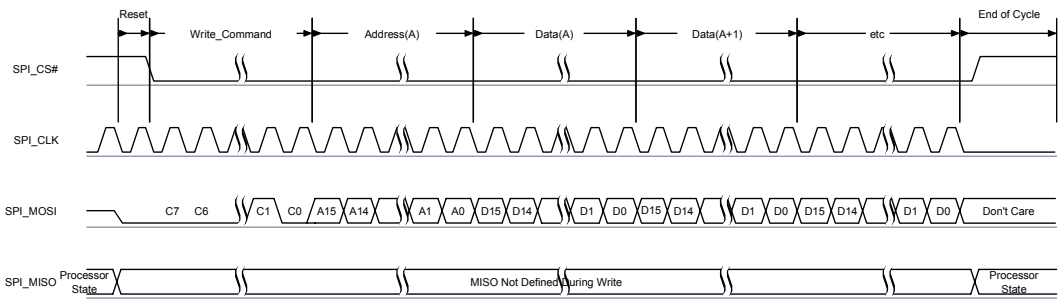


Figure 8.7: SPI Write Operation

8.3.3 Reading from the Device

Reading from BlueCore5-FM WLCSP is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore5-FM WLCSP then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CS# is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CS# is taken high.

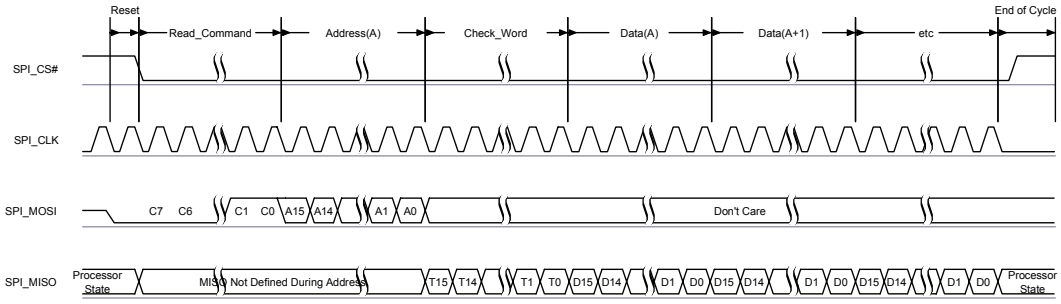


Figure 8.8: SPI Read Operation

8.3.4 Multi-Slave Operation

BlueCore5-FM WLCSP should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore5-FM WLCSP is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BlueCore5-FM WLCSP outputs 0 if the processor is running or 1 if it is stopped.

8.4 I²C Interface

BlueCore5-FM WLCSP supports an I²C interface on dedicated pins, dedicated to FM control.

8.4.1 I²C Operation

I²C operation meets the I²C bus specification for data rates up to 400kbits/s.

The device's I²C address is defined by the configuration key PSKEY_FM_I2C_SLAVE_ADDRESS, which is stored in persistent memory.

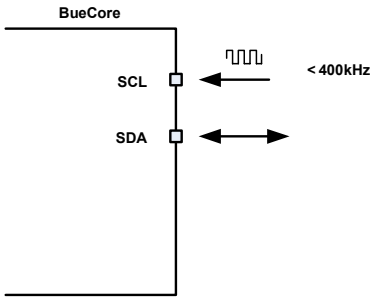


Figure 8.9: I²C Interface Pins

Data is transferred over the I²C in bytes. The first data byte transferred following a start condition is the device address. Following the address, and assuming a write condition, the host transfers a local address to the interface. The next byte transferred by the host is written to this address. The local address auto increments for all subsequent bytes.

Any octets to be transferred over the I²C bus that contain bits with no defined meaning (or bits defined as being reserved) must have those bits zeroed before transmission.

The transaction is completed by either a STOP or RESTART flag from the host.

The FM receiver state is not updated until the last octet in a multiple octet register has been written, but if the I²C sequence is aborted before all octets have been transmitted, the register's value is updated but the tuner's internal state is not. Aborting a multiple octet write I²C sequence should be avoided to prevent this mismatch.

In the case of a read cycle the host must first set up a local address using the same procedure as a write cycle. Following the local address byte the host issues a RESTART and the device address followed by the read flag. The I²C interface responds with data from incrementing addresses beginning with the local address until an inverted acknowledge is received from the host, or a START or STOP flag is received.

Whenever a bit becomes set in the FLAG_GET register, an event is signalled to the host as a pulse on a dedicated physical wire. This interrupt alerts the host which should then read the FLAG register and other registers as appropriate. The transmission of the pulse can be masked with the INT_MASK register on a per-bit basis. See section 5.3 for more details.

The I²C interface always monitors the SCL and SDA lines, even when BlueCore5-FM is in deep sleep.

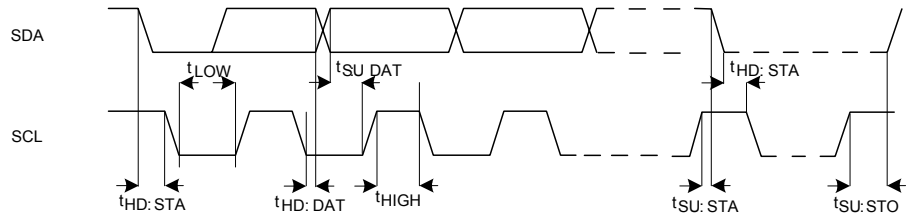


Figure 8.10: I²C Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
-	SCL Frequency	-	-	400	kHz
t_{LOW}	Low Period of SCL Clock	1.3	-	-	µs
t_{HIGH}	High Period of SCL Clock	0.6	-	-	µs
$t_{SU:STA}$	Setup time for a repeated start condition	0.6	-	-	µs
$t_{SU:STO}$	Setup time for a stop condition	0.6	-	-	µs
$t_{SU:DAT}$	Data setup time	100	-	-	ns
$t_{HD:STA}$	Hold time for a repeated start condition	0	-	-	ns
$t_{HD:DAT}$	Data hold time	0	-	0.9	µs

Table 8.5: I²C Interface Timing

8.4.2 Host Interrupt

There is an interrupt flag register which defines the interrupt sources on the I²C interface. Any of the sources defined in the register cause a host interrupt to be generated. Each interrupt source is accompanied by a corresponding mask defined in the interrupt mask register. The interrupt mechanism is shown in Figure 8.11.

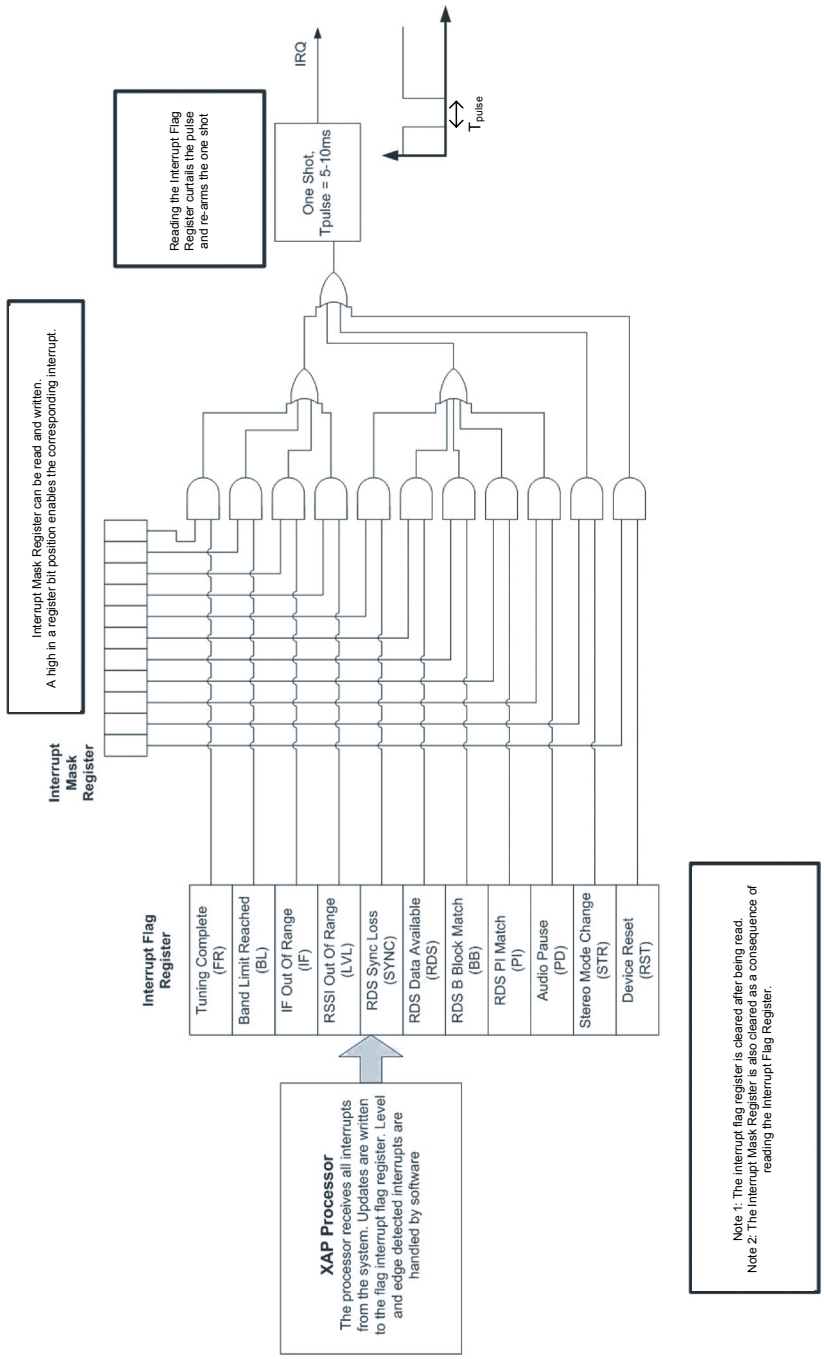


Figure 8.11: Interrupt Mask Register

The host interrupt is triggered when an entry is set in the interrupt flag register by the processor. Each of the interrupt sources are independently masked by clearing the corresponding interrupt entry in the interrupt mask register.

The interrupt flag register is cleared when read from the host. The BlueCore5-FM WLCSP default configuration assigns this signal to PIO[10].

The host interrupt is an active low one shot signal with a programmable duration, which is configured by the processor.

9 Audio Interfaces

9.1 Audio Interface Overview

The audio interface circuit consists of a stereo audio CODEC, dual audio outputs, and a PCM or I²S configurable digital audio interface. Figure 9.1 outlines the functional blocks of the interface. The CODEC supports stereo playback of audio signals at multiple sample rates with a resolution of 16-bit. Any DAC channel can be run at its own independent sample rate.

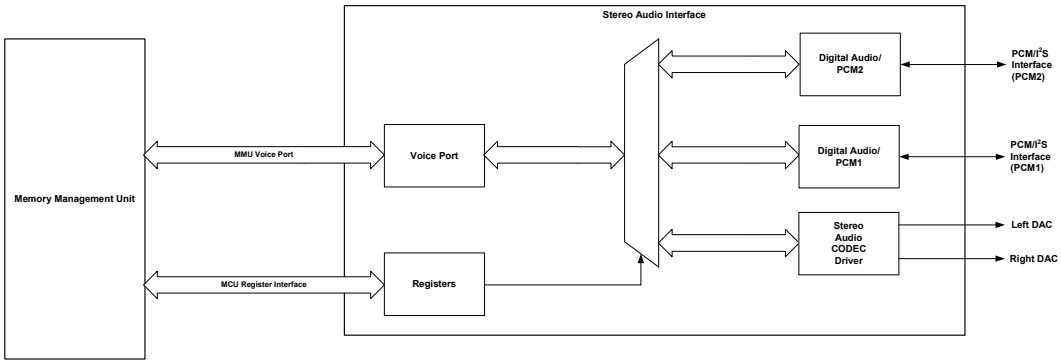


Figure 9.1: Audio Interface

The interface for the digital audio bus shares the same pins as the PCM interface described in section 9.3 which means each of the audio buses are mutually exclusive in their usage. The device diagram in shows the pinout for the PCM interface with alternative pin descriptions. Table 9.1 lists these alternative functions.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 9.1: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

9.1.1 Audio Output

The audio output circuitry consists of a dual class A-B output stage.

9.2 Stereo Audio CODEC Interface

The main features of the interface are:

- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I²S
- Support for IEC-60958 standard stereo digital audio bus standards, e.g. AES3/EBU
- Support for PCM interfaces including PCM master CODECs that require an external system clock

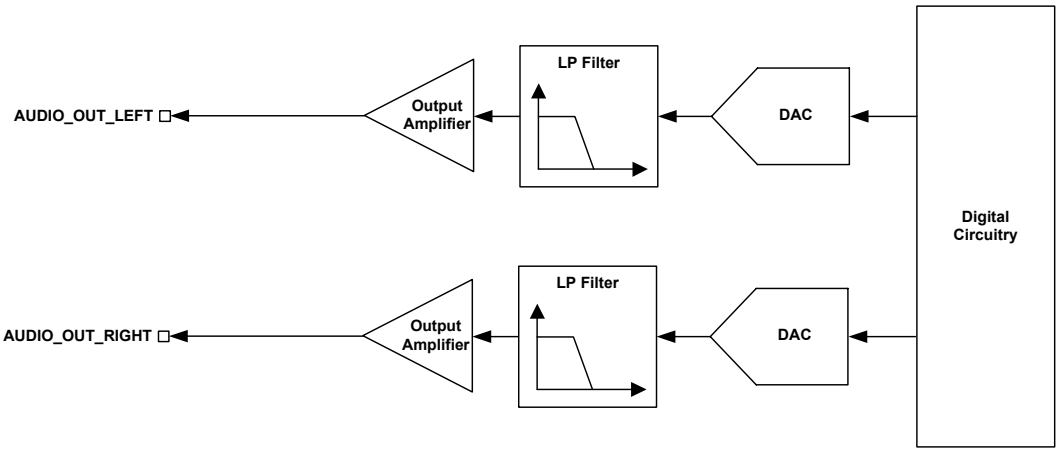


Figure 9.2: Stereo CODEC Audio Input and Output Stages

The stereo audio CODEC operates from a single power-supply of 1.5V and uses a minimum of external components.

Important Note:

To avoid any confusion with respect to stereo operation this data sheet explicitly states which is the left and right channel for audio input and output. With respect to software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel for both input and output.

For mono operation this data sheet uses the left channel for standard mono operation for audio input and output and with respect to software and any registers, channel 0 or channel A represents the standard mono channel for audio input and output. In mono operation the second channel which is the right channel, channel 1 or channel B could be used as a second mono channel if required and this channel will be known as the auxilliary mono channel for audio input and output.

9.2.1 DAC

The DAC consists of two third order Sigma Delta converters allowing two separate channels that are identical in functionality as shown in .

9.2.2 DAC Sample Rate Selection and Warping

Each DAC supports the following samples rates:

- 48kHz
- 44.1kHz
- 32kHz
- 24kHz
- 22.050kHz
- 16kHz
- 11.025kHz
- 8kHz

9.2.3 DAC Gain

The DAC contains two gain stages for each channel: a digital and an analogue gain stage.

The digital gain stage has a programmable selection value in the range of 0 to 15 with associated DAC gain settings.

Gain Selection Value	DAC Digital Gain Setting (dB)
0	0
1	3.5

Gain Selection Value	DAC Digital Gain Setting (dB)
2	6
3	9.5
4	12
5	15.5
6	18
7	21.5
8	-24
9	-20.5
10	-18
11	-14.5
12	-12
13	-8.5
14	-6
15	-2.5

Table 9.2: DAC Digital Gain Rate Selection

9.3 PCM Interface

The audio pulse code modulation (PCM) interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

There are two audio interfaces. Each can be independently configured as an I²S or a PCM port. The PCM1 interface also shares the same physical set of pins with the SPI interface described in section 8.3. Either interface is selected using SPI_PCM#_SEL:

- SPI_PCM#_SEL = 1 selects SPI
- SPI_PCM#_SEL = 0 selects PCM

Important Note:

The PCM description refers to both PCM1 or PCM2.

Pulse Code Modulation (PCM) is a standard method used to digitise audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore5-FM WLCSP has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore5-FM WLCSP offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore5-FM WLCSP allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time.

BlueCore5-FM WLCSP can operate as the PCM interface master generating an output clock of 128, 256, 512, 1536 or 2400kHz. When configured as a PCM interface slave, it can operate with an input clock up to 2400kHz. BlueCore5-FM WLCSP is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG32 (0x1b3).

9.3.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore5-FM WLCSP generates PCM_CLK and PCM_SYNC.

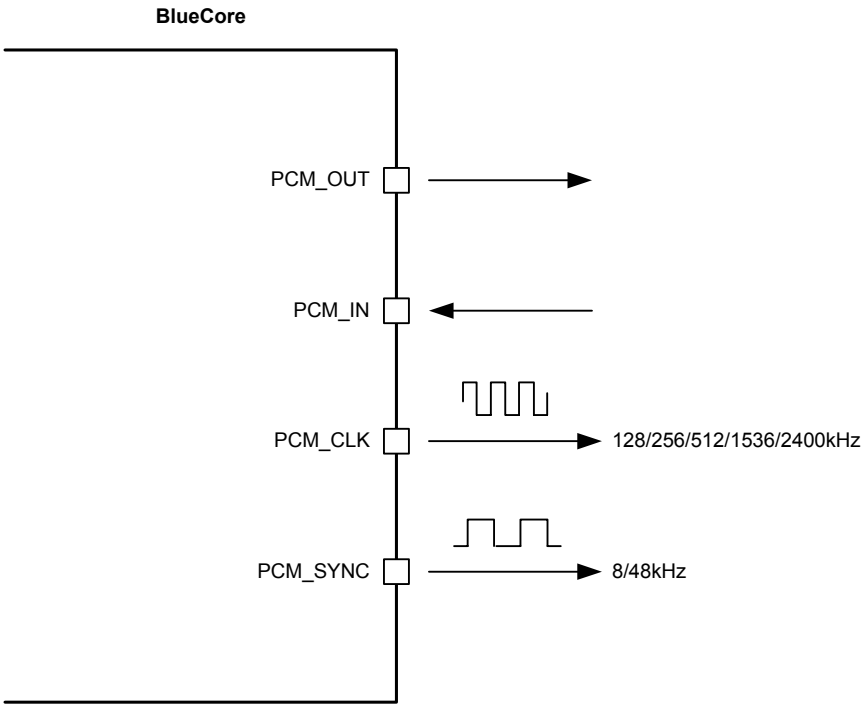


Figure 9.3: PCM Interface Master

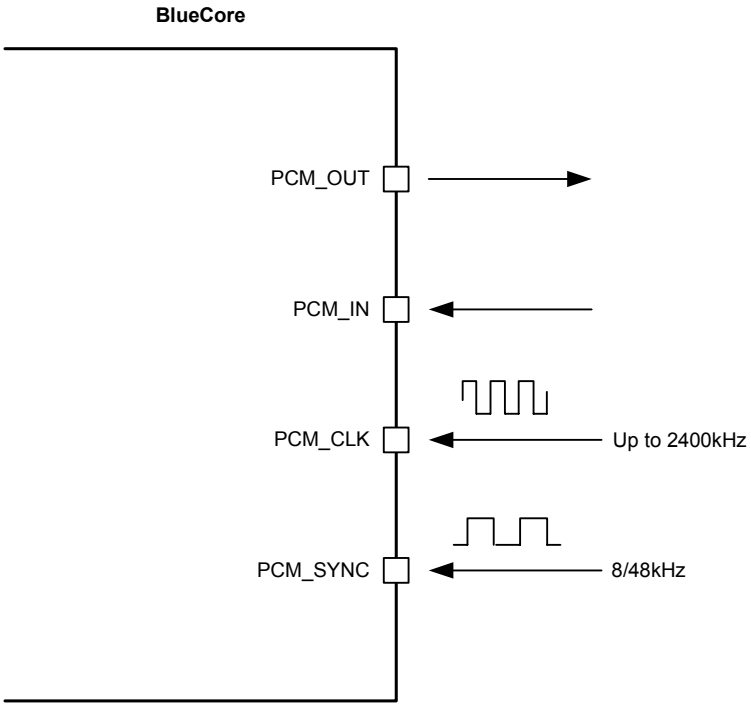


Figure 9.4: PCM Interface Slave

9.3.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore5-FM WLCSP is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8 bits long. When BlueCore5-FM WLCSP is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5µs long.

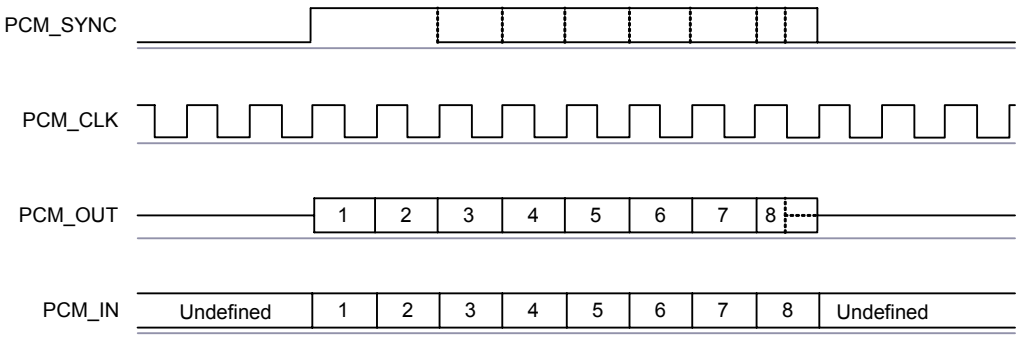


Figure 9.5: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore5-FM WLCSP samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.3.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

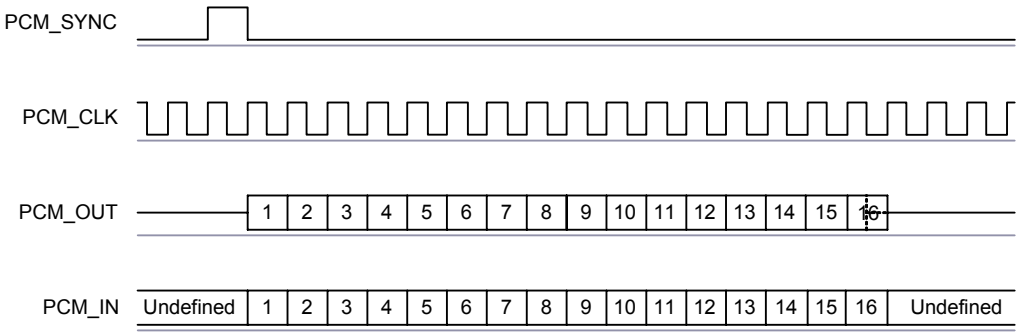


Figure 9.6: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore5-FM WLCSP samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.3.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

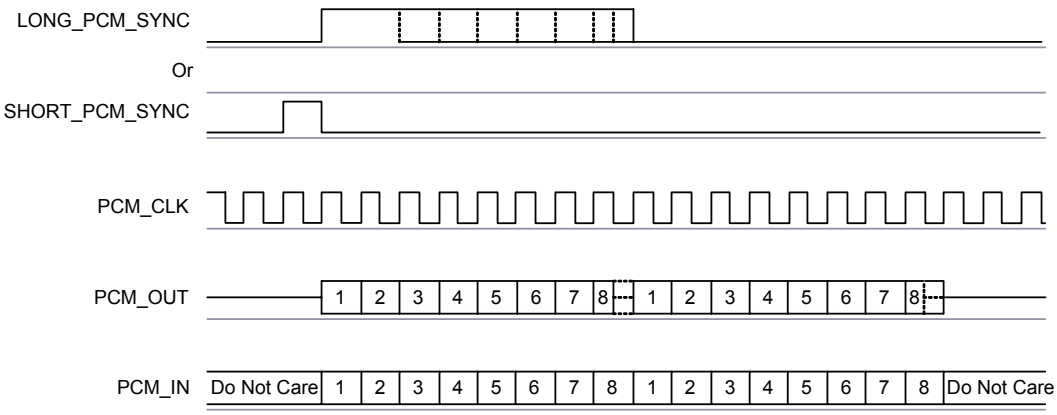


Figure 9.7: Multi-slot Operation with Two Slots and 8-bit Companded Samples

9.3.5 GCI Interface

BlueCore5-FM WLCSP is compatible with the General Circuit Interface (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64kbps B channels can be accessed when this mode is configured.

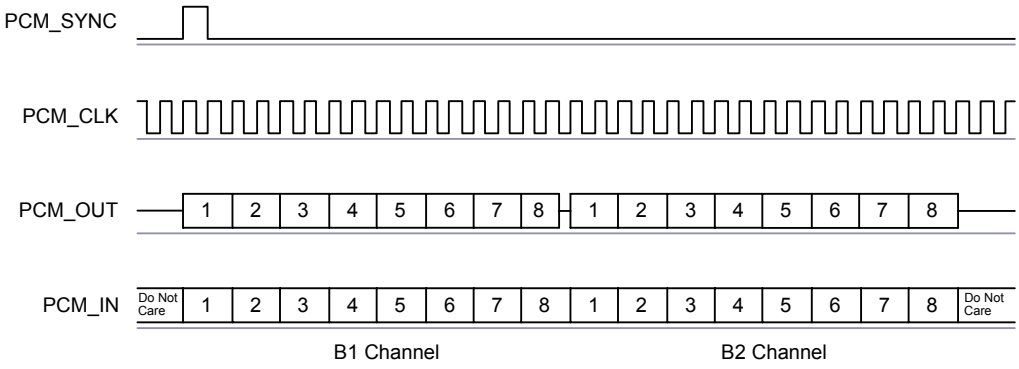


Figure 9.8: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore5-FM WLCSP in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

9.3.6 Slots and Sample Formats

BlueCore5-FM WLCSP can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore5-FM WLCSP supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

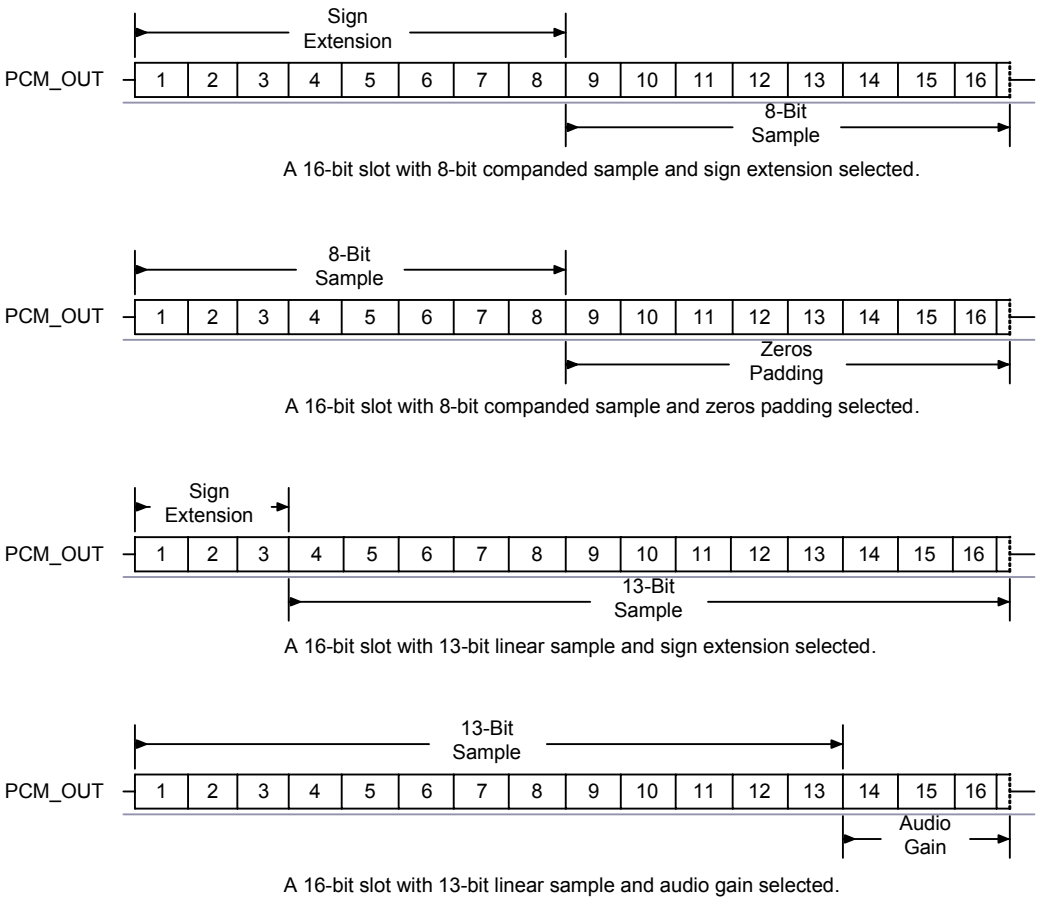


Figure 9.9: 16-Bit Slot Length and Sample Formats

9.3.7 Additional Features

BlueCore5-FM WLCSP has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

9.3.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 9.6.	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable. See Table 9.5 and PCM_CLK and PCM_SYNC Generation on page 48.	2.9	-	-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh}[(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl}[(a)]	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 9.3: PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

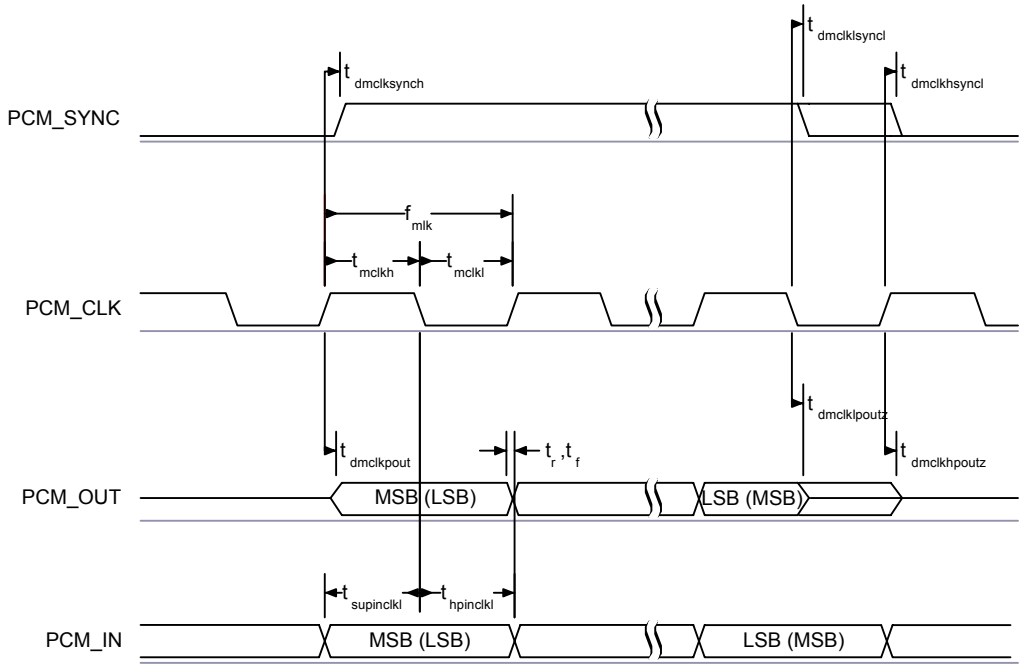


Figure 9.10: PCM Master Timing Long Frame Sync

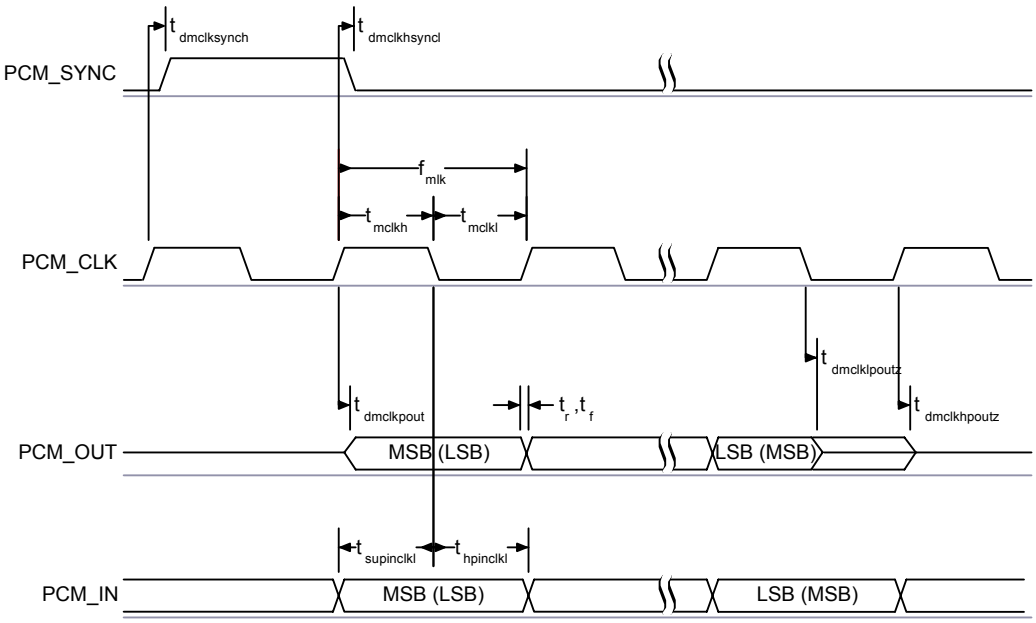


Figure 9.11: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 9.4: PCM Slave Timing

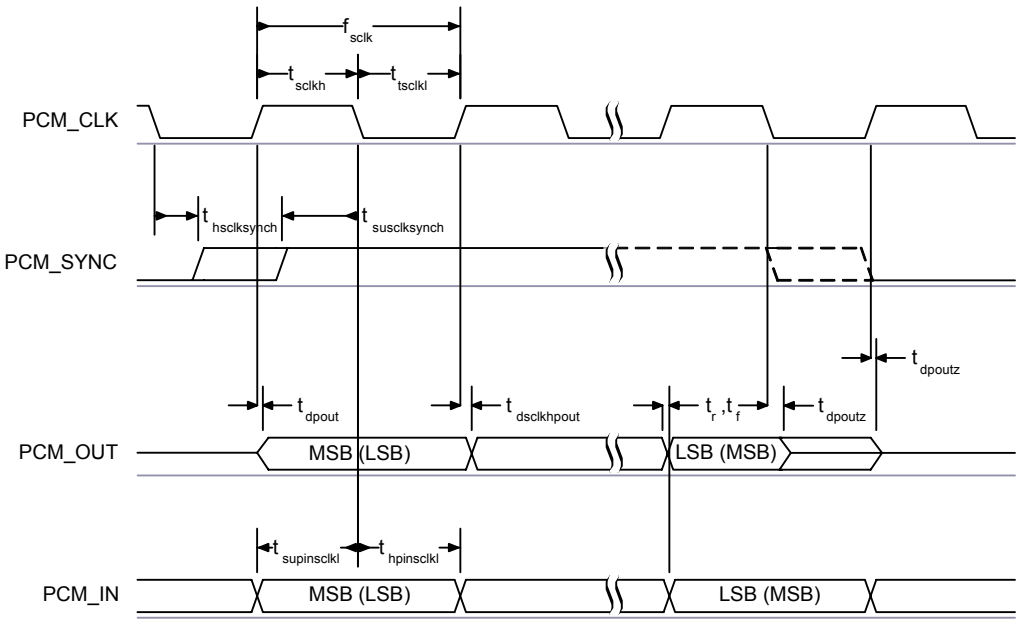


Figure 9.12: PCM Slave Timing Long Frame Sync

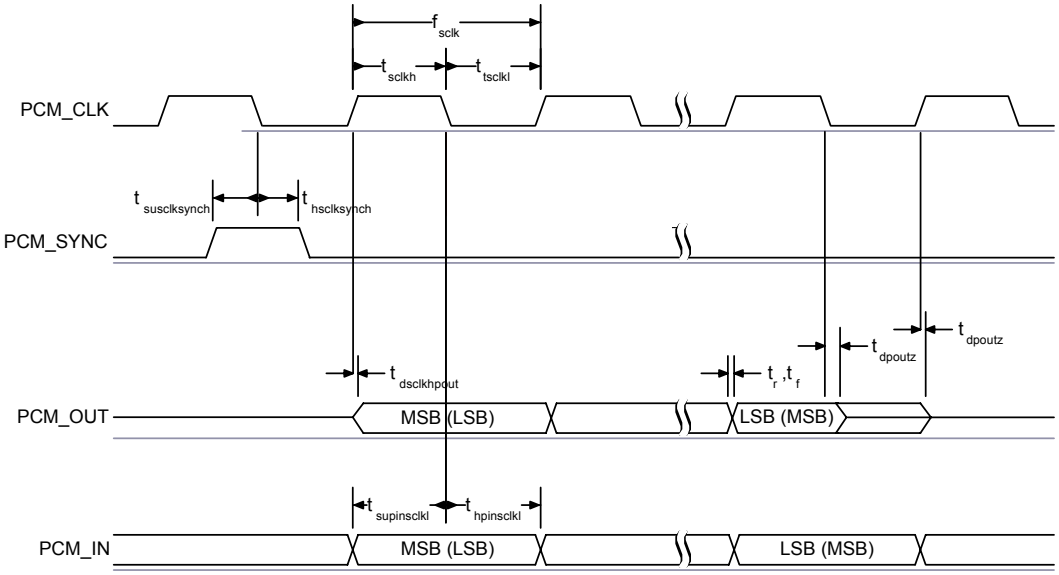


Figure 9.13: PCM Slave Timing Short Frame Sync

9.3.9 PCM_CLK and PCM_SYNC Generation

BlueCore5-FM WLCSP has two methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by Direct Digital Synthesis (DDS) from BlueCore5-FM WLCSP internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 9.1 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 9.1: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

Set the frequency of PCM_SYNC relative to PCM_CLK using Equation 9.2 dependent on the setting of PCM_SYNC_MULT (see Table 9.7). If set:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT} \qquad f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 9.2: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

9.3.10 PCM Configuration

The PCM configuration is set using the PS Keys, PSKEY_PCM_CONFIG32 described in Table 9.6, PSKEY_PCM_LOW_JITTER_CONFIG in Table 9.5, and PSKEY_PCM_SYNC_MULT in Table 9.7. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT.

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 9.5: PSKEY_PCM_LOW_JITTER_CONFIG Description

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tri-state PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC while keeping PCM_CLK running. Some CODECS use this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode.
MUTE_EN	10	1 = force PCM_OUT to 0.

Name	Bit Position	Description
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16-cycle slot duration or 8 (0b11) bit sample with 8-cycle slot duration.

Table 9.6: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
PCM_SYNC_MULT	12	0 - Sync limit = SYNC_LIMIT x 8 1 - SYNC_LIMIT

Table 9.7: PSKEY_PCM_SYNC_MULT Description

9.4 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified (LJ) or right-justified(RJ). The interface shares the same pins as the PCM interface as shown in section 3.2, which means each audio bus is mutually exclusive in its usage. Table 9.8 lists these alternative functions. Figure 9.14 shows the timing diagram.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 9.8: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Table 9.9 describes the values for the PS Key (PSKEY_DIGITAL_AUDIO_CONFIG) that sets up the digital audio interface. For example, to configure an I²S interface with 16-bit SD data set PSKEY_DIGITAL_CONFIG to 0x0406.

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17 bit SD data is rounded down to 16 bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00F0	CONFIG_AUDIO_ATTEN	Attenuation in 6 dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16 bit, 01= 20 bit, 10=24 bit, 11=Reserved. This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17 bit SD_IN data is rounded down to 16 bits. For 1 only the most significant 16 bits of data are received.

Table 9.9: PSKEY_DIGITAL_AUDIO_CONFIG

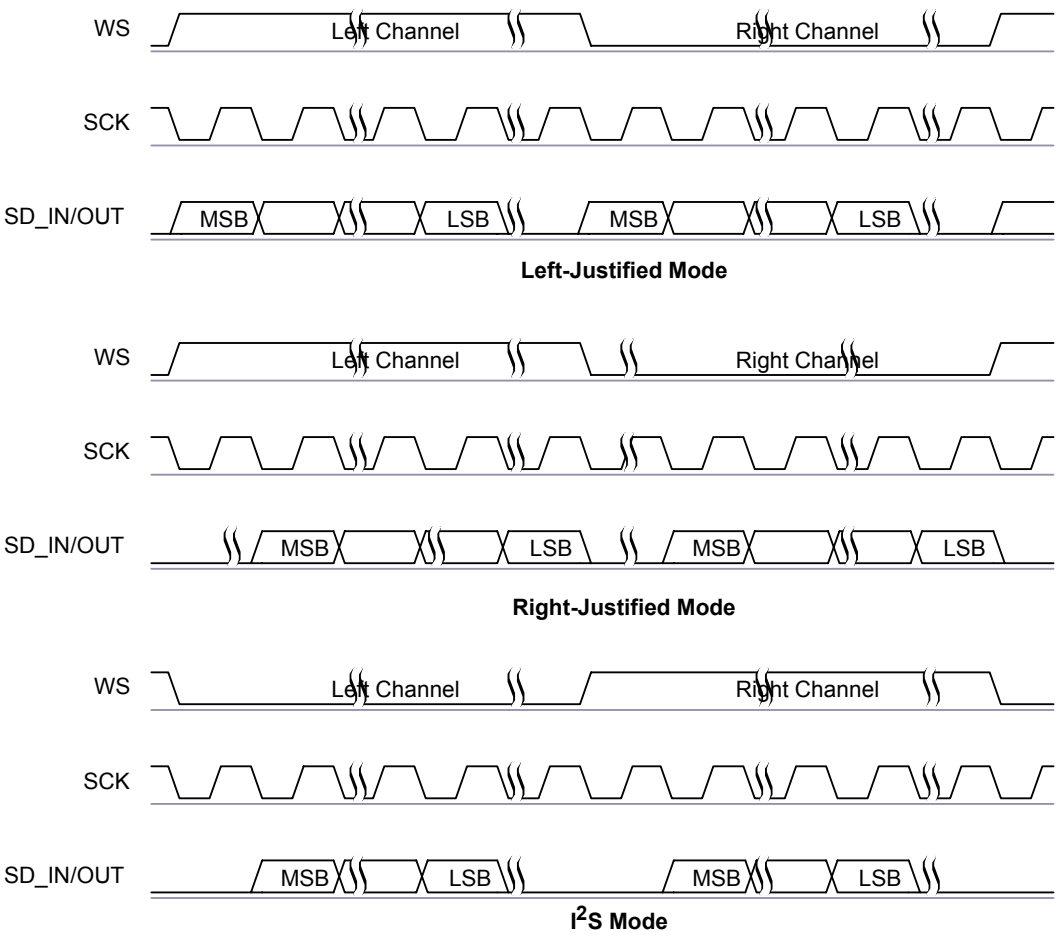


Figure 9.14: Digital Audio Interface Modes

The internal representation of audio samples within BlueCore5-FM WLCSP is 16-bit and data on SD_OUT is limited to 16-bit per channel. On SD_IN, if more than 16-bit per channel is present will round considering the 17th bit.

SCK typically operates 64 x WS frequency and cannot be less than 36 x WS.

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{ssu}	WS to SCK high set-up time	20	-	-	ns
t_{sh}	WS to SCK high hold time	20	-	-	ns
t_{isu}	SD_IN to SCK high set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK high hold time	20	-	-	ns

Table 9.10: Digital Audio Interface Slave Timing

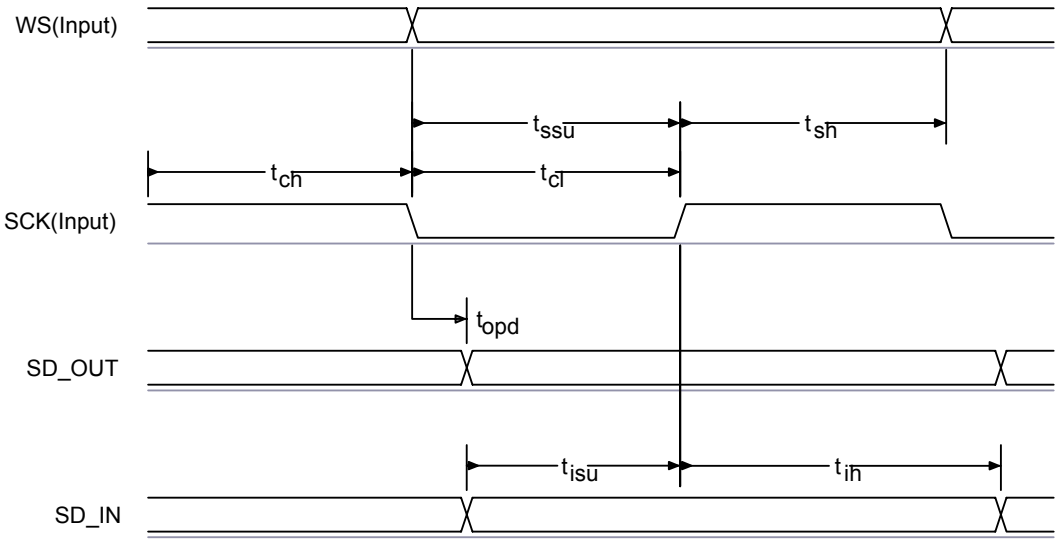


Figure 9.15: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{spd}	SCK to WS delay	-	-	-	ns
t_{isu}	SD_IN to SCK high set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK high hold time	10	-	-	ns

Table 9.11: Digital Audio Interface Master Timing

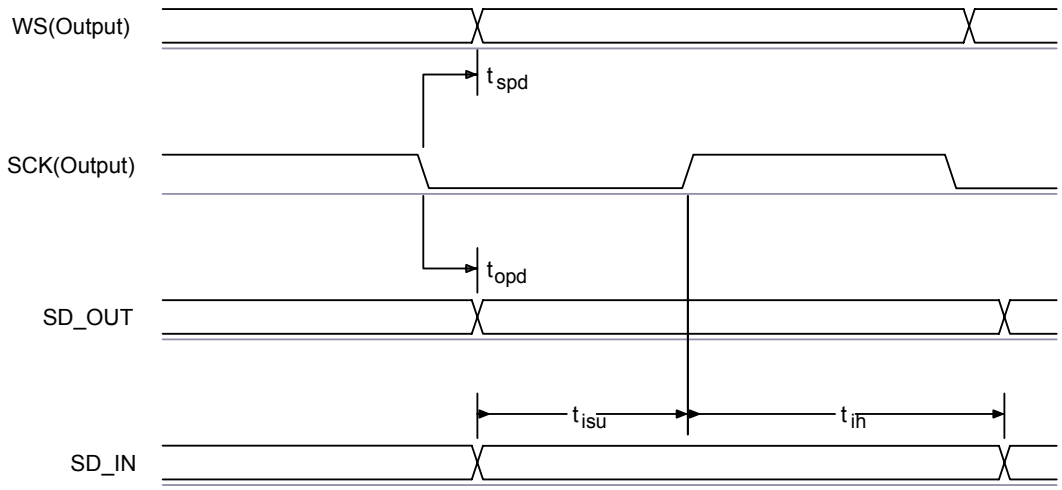


Figure 9.16: Digital Audio Interface Master Timing

10 Power Control and Regulation

10.1 Power Control and Regulation

BlueCore5-FM WLCSP contains two linear regulators:

- A high voltage regulator to generate a 1.8V rail for the chip I/Os
- A low-voltage regulator to supply the 1.5V core supplies from the 1.8V rail.

The chip can be powered from a high-voltage rail through both regulators, as shown in Figure 10.1. Alternatively the chip can be powered directly from an external 1.8V rail, bypassing the high- voltage regulator, or from an external 1.5V rail omitting both regulators.

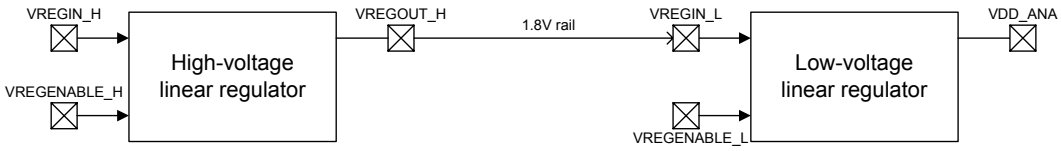


Figure 10.1: Voltage Regulator Configuration

10.2 Sequencing

The 1.5V supplies are VDD_ANA, VDD_RADIO, VDD_CORE, VDD_FM and VDD_AUDIO. CSR recommends that the 1.5V supplies are all powered at the same time. The order of powering the 1.5V supplies relative to the other I/O supplies (VDD_PIO, VDD_PADS, VDD_DIG) is not important. However, if the I/O supplies are powered before the 1.5V supplies .

VDD_ANA, VDD_RADIO, VDD_FM and VDD_AUDIO should be connected directly to the 1.5V supply; a simple RC filter is recommended for VDD_CORE to reduce transients fed back onto the power supply rails.

The I/O supplies may be connected together or independently to supplies at an appropriate voltage. They should be simply decoupled.

10.3 External Voltage Source

If the 1.5V rails of BlueCore5-FM WLCSP are supplied from an external voltage source, CSR recommends that VDD_RADIO, VDD_ANA, VDD_FM and VDD_AUDIO should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided.

The transient response of any regulator used should be 20µs or less. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels (refer to the average current consumption specification of the regulator).

10.4 High-voltage Linear Regulator

The on-chip high-voltage regulator may be used to power a 1.8V rail which can drive the chip I/O supplies, and the input to the low voltage regulator. A smoothing circuit using a 2.2µF low ESR capacitor and a 2.2Ω resistor to ground should be connected to the output of the regulator VREGOUT_H. Alternatively a 2.2µF capacitor with at least 2Ω ESR may be used. See the Application Schematic in section 11.

This regulator may be disabled by holding the VREGENABLE_H pin low. This pin has an internal weak pull-down to disable the regulator if VREGENABLE_H is not connected.

The regulator is switched into a low power mode when the device is in deep-sleep mode, or in reset.

When this regulator is not used the terminals VREGIN_H and VREGOUT_H must be left unconnected, or tied to ground.

10.5 Low-voltage Linear Regulator

The on-chip low-voltage regulator may be used to power the 1.5V supplies. The output of this regulator is connected internally to VDD_ANA, and must be connected externally to the other 1.5V supply pads. A smoothing circuit using a 2.2µF low ESR capacitor and a 2.2Ω resistor to ground should be connected to the output of the regulator. Alternatively a 2.2µF capacitor with at least 2.0Ω ESR may be used. See the Application Schematic in .

This regulator may be disabled by holding the VREGENABLE_L pin low. This pin has an internal weak pull-down to disable the regulator if VREGENABLE_L is not connected.

The regulator is switched into a low power mode when the device is in deep-sleep mode, or in reset.

When this regulator is not used the terminal VREGIN_L must be left unconnected, or tied to VDD_ANA.

10.6 VREGENABLE Pins

The regulator enable pins, VREGENABLE_H and VREGENABLE_L, are used to enable and disable the BlueCore5-FM WLCSP device if the on-chip regulators are being used. VREGENABLE_H enables the high-voltage regulator; VREGENABLE_L enables the low-voltage regulator.

Both pins are active high, with a logic threshold of around 1V, and both have weak pull-downs. They can tolerate voltages up to 4.9V, so both pins may be connected directly to a battery to enable the device.

The status of the VREGENABLE_H pin is available to firmware through an internal connection. VREGENABLE_H also works as an input line.

10.7 Reset (RST#)

BlueCore5-FM WLCSP may be reset from several sources:

- RST# pin
- power-on reset
- a UART break character
- via a software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low-frequency clock oscillator. A reset is performed between 1.5 and 4.0ms following RST# being active. CSR recommends that RST# is applied for a period greater than 5ms.

The power on reset occurs when the VDD_CORE supply falls below typically 1.26V and is released when VDD_CORE rises above typically 1.31V. At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The pull-down state is shown in Table 10.1. Following a reset, BlueCore5-FM WLCSP assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore5-FM WLCSP is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore5-FM WLCSP free runs, again at a safe frequency.

10.7.1 Digital Pin States on Reset

The digital I/O drivers for BlueCore5 family devices are based on a common pad sub-circuit, which is a fully configurable bi-directional pad with the following capabilities for both bus-keeper and non-bus keeper pins:

- The pad can behave as an input buffer or an output driver.
- When in input mode, the pull direction is specified as one of either strong pull-up, weak pull-up, strong pull-down or weak pull-down.
- When no core voltage is present, the pull direction can be determined as one of either strong pull-up, weak pull-up, strong pull-down or weak pull-down.
- When in input mode, configurable pads can have the pull resistor disabled after reset. This disable over-ride has no affect on the weak pull down at the input pads when no core voltage is present.
- To improve flexibility, a bus keeper mode is available on all communication interfaces during normal operation. When enabled by firmware through a configuration register defined by a PS Key, this mode causes the direction of the pull-resistor to follow the polarity of the signal being driven into the input. In this mode, the pull can still be selected to be either strong or weak. The PS Key is to be defined. For full information on PS Keys refer to the Release Note and the firmware.

Table 10.2 and Table 10.3 show the pin states of BlueCore5-FM WLCSP on reset for bus-keeper and non-bus keeper pads. Pull-up (PU) and pull-down (PD) default to weak values unless specified otherwise.

Pin Name / Group	I/O Type	No Core Voltage Reset		Full Chip Reset		Configurable After Reset	Bus Keeper Group
		Pull R	I/O	Pull R	I/O		
Reset/Control							
RST#	Digital input	PU	Input	PU	Input	Y	RESET

Table 10.1: Pin States of BlueCore5-FM WLCSP on Reset

Pin Name / Group	I/O Type	No Core Voltage Reset		Full Chip Reset		Configurable After Reset	Bus Keeper Group
		Pull R	I/O	Pull R	I/O		
Digital Interfaces - UART							
UART_RX	Digital input	PD	Input	PU	Input	Y	UART
UART_TX	Digital bi-directional	PU	Input	PU	Input	Y	UART
UART_CTS	Digital input	PD	Input	PU	Input	Y	UART
UART_RTS	Digital bi-directional	PU	Input	PU	Input	Y	UART
Digital Interfaces - USB							
USB_DP	Bi-directional selectable PU input	-	-	-	-	N	N/a
USB_DN	Bi-directional selectable PU input	-	-	-	-	N	N/a

Pin Name / Group	I/O Type	No Core Voltage Reset		Full Chip Reset		Configurable After Reset	Bus Keeper Group
		Pull R	I/O	Pull R	I/O		
PCMs							
PCM1_IN	Digital	PD	Input	PD	Input	Y	PCM1
PCM1_OUT	Digital tri-state output	PD	Input	PD	High impe-dance	Y	PCM1
PCM1_CLK	Digital bi-directional	PD	Input	PD	Input	Y	PCM1
PCM1_SYNC	Digital bi-directional	PD	Input	PD	Input	Y	PCM1
PCM2_IN	Digital input	PD	Input	PD	Input	Y	PCM2
PCM2_OUT	Digital output	PD	Input	PD	Input	Y	PCM2
PCM2_CLK	Digital bi-directional	PD	Input	PD	Input	Y	PCM2
PCM2_SYNC	Digital bi-directional	PD	Input	PD	Input	Y	PCM2

Pin Name / Group	I/O Type	No Core Voltage Reset		Full Chip Reset		Configurable After Reset	Bus Keeper Group
		Pull R	I/O	Pull R	I/O		
SPI Interface							
SPI_MOSI	Digital input	PD	Input	PD	Input	Y	SPI
SPI_CLK	Digital bi-directional	PD	Input	PD	Input	Y	SPI
SPI_CS#	Digital input	PD	Input	PD	Input	Y	SPI
SPI_MISO	Digital tri-state output	PD	Input	PD	Input	Y	SPI

Pin Name / Group	I/O Type	No Core Voltage Reset		Full Chip Reset		Configurable After Reset	Bus Keeper Group
		Pull R	I/O	Pull R	I/O		
I^2C							
I2C_CLK	Digital input	PU	Input	PU	Input	Y	I^2C
I2C_DATA	Digital output	PU	Input	PU	Input	Y	I^2C

Pin Name / Group	I/O Type	No Core Voltage Reset		Full Chip Reset		Configurable After Reset	Bus Keeper Group
		Pull R	I/O	Pull R	I/O		
PIOs							
PIO[0]	Digital bi-directional	PD	Input	PD	Input	Y	PIO_0
PIO[1]	Digital bi-directional	PD	Input	PD	Input	Y	PIO_1
PIO[2]	Digital bi-directional	PD	Input	PD	Input	Y	PIO_2
PIO[3]	Digital bi-directional	PD	Input	PD	Input	Y	PIO_3
PIO[4]	Digital bi-directional	PD	Input	PD	Input	Y	PIO_4
PIO[5]	Digital bi-directional	PD	Input	PD	Input	Y	PIO_5
PIO[6]	Digital bi-directional	PD	Input	PD	Input	Y	PIO_6
PIO[7]	Digital bi-directional	PD	Input	PD	Input	Y	PIO_7
PIO[8]	Digital bi-directional	PD	Input	PD	Input	Y	PIO_8
PIO[9]	Digital bi-directional	PD	Input	PD	Input	Y	PIO_9

Pin Name / Group	I/O Type	No Core Voltage Reset		Full Chip Reset		Configurable After Reset	Bus Keeper Group
		Pull R	I/O	Pull R	I/O		
PIO[10]	Digital bi-directional	PU	Input	PU	Input	Y	PIO_10

Table 10.2: Pin States of BlueCore5-FM WLCSP on Reset in Bus Keeper Group

Pin Name / Group	I/O Type	During Reset		Full Chip Reset		Configurable After Reset
		Pull R	I/O	Pull R	I/O	
Clocking						
XTAL_IN	Ref clock	None	Input	None	Input	N
4-Wire						
SPI_PCM#_SEL	Digital input	PD	Input	PD	Input	N
FM Receiver (Analogue)						
Left Audio	Audio	None	Output	None	Output	N
Right Audio	Audio	None	Output	None	Output	N
Test						
TEST_EN	Digital input	Strong PD	Input	Strong PD	Input	N

Table 10.3: Pin States of BlueCore5-FM WLCSP on Reset Not in Bus Keeper Group

Table 10.5 and Table 10.5 show the PS Keys that control "bus-keeper" mode and "pull-disable" mode.

PS Key	Digital Interface	Effective	Activated	De-activated
PSKEY_BCSP_PULL _CONTROL[(a)]	UART	UART_RX, UART_TX, UART_CTS, UART_RTS	At boot time, during BCSP/H5 initialisation, when BCSP or H5 are selected as the host transport	No
PSKEY_H4DS_PULL _CONTROL	UART	UART_RX, UART_TX, UART_CTS, UART_RTS	At boot time, during H4DS initialisation, when H4DS is selected as the host transport	No
PSKEY_PCM_PULL_ CONTROL	PCM1 and PCM2	PCMx_IN, PCMx_OUT, PCMx_CLK and PCMx_SYNC	During PCM or I2S data transfer	On completion of data transfer
			At boot time	No
PSKEY_LC_COMBO _DOT11_ PULL _CONTROL	PIOs	PIO[xx]	At boot time, when WLAN co-existence is implemented	No
PSKEY_FM_I2C_SLAVE_ PULL_CONTROL	I2C	I2C_CLK, I2C_DATA	If I2C interface is enabled at boot time	No
PSKEY_DEEP_SLEEP _EXTERNAL_CLOCK_ PULL_CONTROL	SLEEP_CLK	SLEEP_CLK	At boot time when an external 32.768kHz reference clock is used	No

PS Key	Digital Interface	Effective	Activated	De-activated
PSKEY_MISC_PULL_CONTROL	Misc (Reset, SPI)	RST#, SPI_MOSI, SPI_MISO, SPI_CLK, SPI_CS#	At boot time when an external 32.768kHz reference clock is used	No

Table 10.4: Pull Control

(a) For full information on PS Keys refer to the Release Note and the firmware.

PS Key		Description	Polarity	
			0	1
PSKEY_BCSP_PULL_CONTROL(a)				
Bit	0	Controls bus-keeper mode of operation	Disabled	Enabled(b)
	1	Controls pull-disable mode of operation	Disabled	Enabled
PSKEY_H4DS_PULL_CONTROL				
Bit	0	Controls bus-keeper mode of operation	Disabled	Enabled
	1	Controls pull-disable mode of operation	Disabled	Enabled
PSKEY_PCM_PULL_CONTROL				
Bit	0	Controls bus-keeper mode of operation on PCM1	Disabled	Enabled
	1	Controls pull-disable mode of operation on PCM1	Disabled	Enabled
	2(c)	Controls bus-keeper mode of operation on PCM1	Disabled	Enabled and never disabled
	3(b)	Controls pull-disable mode of operation on PCM1	Disabled	Enabled and never disabled
	4	Controls bus-keeper mode of operation on PCM2	Disabled	Enabled
	5	Controls pull-disable mode of operation on PCM2	Disabled	Enabled
	6(b)	Controls bus-keeper mode of operation on PCM2	Disabled	Enabled and never disabled
	7(b)	Controls pull-disable mode of operation on PCM2	Disabled	Enabled and never disabled
PSKEY_LC_COMBO_DOT11_PULL_CONTROL				
Bit	0	Controls bus-keeper mode	Disabled	Enabled
	1	Controls pull-disable mode	Disabled	Enabled
PSKEY_FM_I2C_SLAVE_PULL_CONTROL				
Bit	0	Controls bus-keeper mode of operation	Disabled	Enabled
	1	Controls pull-disable mode of operation	Disabled	Enabled
PSKEY_DEEP_SLEEP_ EXTERNAL_CLOCK_PULL_CONTROL				
Bit	0	Controls bus-keeper mode of operation	Disabled	Enabled
	1	Controls pull-disable mode of operation	Disabled	Enabled
PSKEY_MISC_PULL_CONTROL				

PS Key		Description	Polarity	
			0	1
Bit	0	Controls bus-keeper mode of operation: RST#	Disabled	Enabled
	1	Controls pull-disable mode of operation: RST#	Disabled	Enabled
	2	Controls bus-keeper mode of operation: SPI_	Disabled	Enabled
	3	Controls pull-disable mode of operation: SPI_	Disabled	Enabled

Table 10.5: PS Key Bit Descriptions

(a) For full information on PS Keys refer to the Release Note and the firmware.
(b) See Table 10.4
(c) Take effect at boot time

10.7.2 Status after Reset

The chip status after a reset is as follows:

- Warm reset: data rate and RAM data remain available
- Cold reset: data rate and RAM data not available. One of:
  - Power cycle
  - System reset (firmware fault code)
  - Reset signal

11 Example Application Schematic

Note:

This data sheet is Advance Information and CSR may change this example application schematic without notice.

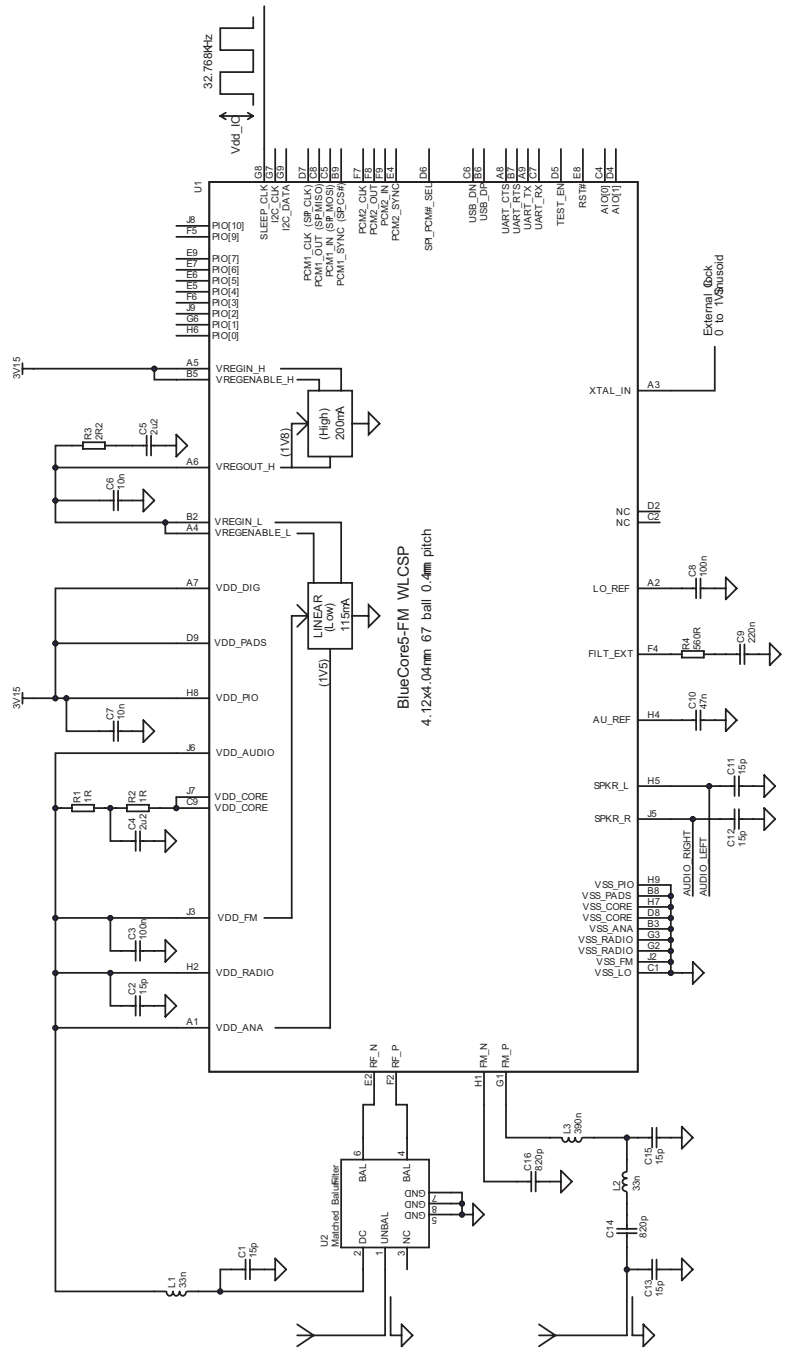


Figure 11.1: Application Schematic for BC5-FM WLCSP

12 Electrical Characteristics

12.1 Absolute Maximums

Rating	Min	Max
Storage temperature	-40°C	+85°C
Core supply voltage: VDD_RADIO, VDD_AUDIO, VDD_FM, VDD_ANA and VDD_CORE	-0.4V	1.65V
I/O supply voltage: VDD_PIO, VDD_PADS and VDD_DIG	-0.4V	3.6V
I/O supply voltage: VREGIN_H, VREGENABLE_H and VREGENABLE_I	-0.4V	4.9V
Other terminal voltages	VSS-0.4V	VDD+0.4V
Voltage swing at FM input pin (RMS)	N/a	400mV

12.2 Recommended Operating Conditions

Operating Condition	Min	Max
Operating temperature range	-30°C	+85°C
Core supply voltage: VDD_RADIO, VDD_AUDIO, VDD_FM, VDD_ANA and VDD_CORE	1.4V	1.6V
I/O supply voltage: VDD_PIO, VDD_PADS and VDD_DIG	1.7V	3.6V

12.3 Input/Output Terminal Characteristics

Notes:

VDD_CORE, VDD_RADIO, VDD_FM, VDD_ANA and VDD_AUDIO are at 1.5V unless shown otherwise.

VDD_PADS, VDD_PIO and VDD_DIG are at 1.8V unless shown otherwise.

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

12.3.1 Linear Regulator, High Voltage

Normal Operation	**Min**	**Typ**	**Max**	**Unit**
Output voltage[a] (I_{load} = 100mA / VREG_IN = 3.0V)	1.7	1.8	1.9	V
Temperature Coefficient	-250	-	+250	ppm/°C
Output noise[b] [c]	-	-	1	mV rms
Load regulation (I_{load} < 100mA)	-	-	50	mV/A
Settling time[b] [d]	-	-	50	µs
Maximum output current	100	-	-	mA
Minimum load current	5	-	-	µA
Input voltage	2.5	-	5.5[e]	V
Dropout voltage (I_{load} = 100mA)	-	-	600	mV
Quiescent current (excluding load, I_{load} < 1mA)	30	40	60	µA
Low Power Mode[f]				
Quiescent current (excluding load, I_{load} < 100µA)	10	13	21	µA
Standby Mode[g]				
Quiescent current	1.5	2.5	3.5	µA

(a) For optimum performance, the VDD_ANA ball adjacent to VREG_IN should be used for regulator output,

(b) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

(c) Frequency range is 100Hz to 100kHz.

(d) 1mA to 100mA pulsed load.

(e) Short-term operation up to 5.5V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore5-FM, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.9V. 5.5V can only be tolerated for short periods.

(f) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.

(g) Regulator is in standby when VREGENABLE_H is pulled low.

12.3.2 Linear Regulator, Low Voltage

Normal Operation	Min	Typ	Max	Unit
Output voltage[a] (I_{load} = 100mA / VREG_IN = 1.7V)	1.4	1.5	1.6	V
Temperature coefficient	-250	-	+250	ppm/°C
Output noise[b] [c]	-	-	1	mV rms
Load regulation (I_{load} < 100mA)	-	-	50	mV/A
Settling time[b] [d]	-	-	50	µs
Maximum output current	100	-	-	mA
Minimum load current	5	-	-	µA
Input voltage	1.7	-	3.15	V
Dropout voltage (I_{load} = 70 mA)	-	-	200	mV
Quiescent current (excluding load, I_{load} < 1mA)	50	90	150	µA
Low Power Mode[e]				
Quiescent current (excluding load, I_{load} < 100µA)	6	10	17	µA
Standby Mode[f]				
Quiescent current	1.5	2.5	3.5	µA

(a) For optimum performance, the VDD_ANA ball adjacent to VREG_IN should be used for regulator output,
(b) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.
(c) Frequency range is 100Hz to 100kHz.
(d) 1mA to 100mA pulsed load.
(e) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.
(f) Regulator is in standby when VREGENABLE_L is pulled low. It is also in standby when VREGIN_L is either open circuit or driven to the same voltage as VDD_ANA.

12.3.3 Digital

Digital Terminals	Min	Typ	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low 1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage Levels				
V_{OL} output logic level low, (I_o = 4.0mA), 1.7V ≤ VDD ≤ 1.9V	-	-	0.4	V
V_{OH} output logic level high, (I_o = -4.0mA), 1.7V ≤ VDD ≤ 1.9V	VDD-0.4	-	-	V
Input and Tri-state Current with:				
Strong pull-up	-100	-40	-10	µA
Strong pull-down	+10	+40	+100	µA
Weak pull-up	-5.0	-1.0	-0.2	µA
Weak pull-down	+0.2	+1.0	+5.0	µA
I/O pad leakage current	-1	0	+1	µA
C_I input capacitance	1.0	-	5.0	pF

12.3.4 Clock

Clock Source	Min	Typ	Max	Unit
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	≤4	-	pF

12.3.5 Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.13	1.25	1.30	V
VDD_CORE rising threshold	1.20	1.30	1.35	V
Hysteresis	0.05	0.10	0.15	V

12.3.6 ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range (LSB size = VDD_ANA/1024)		0	-	VDD_ANA	V
Accuracy	INL	-1	-	+1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-4	-	+4	LSB
Gain Error		-0.2	-	0.2	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.75	-	µs
Sample rate		-	-	700	Samples/s

12.3.7 Sleep Clock

The external sleep clock can be used to replace the internal sleep clock, used for controlling deep sleep modes and the watchdog. When an external slow clock is available, it can also be used to clock the FM radio and audio subsystems without the chip requesting an external crystal clock, and therefore saving power.

Parameter	Conditions/ Notes	Specification			Units
		Min	Nom	Max	
Frequency		32748	32768	32788	Hz
Frequency deviation	-20°C to 85°C	-	-	200	±ppm
Input high level	Square wave	0.625 x VDD_PADS	-	-	V
Input low level	Square wave	-	-	0.425 x VDD_PADS	V
Duty cycle	Square wave	30	-	70	%
Rise and fall time		-	-	50	ns
Integrated frequency jitter	Integrated over the band 200Hz to 15kHz	-	-	-	Hz (rms)

12.4 Power Consumption

Bluetooth Operation Mode[a] [b]	Connection Type	Average	Unit
Page scan, time interval 1.28s	-	0.50	mA
Inquiry and page scan, time interval 1.28s	-	0.86	mA
ACL no traffic	Master	6.4	mA
ACL with file transfer	Master	11	mA
ACL 40ms sniff	Master	1.5	mA
ACL 1.28s sniff	Master	0.19	mA
SCO HV1	Master	34	mA
SCO HV3	Master	17	mA
SCO HV3 30ms sniff	Master	18	mA
ACL no traffic	Slave	14	mA
ACL with file transfer	Slave	17	mA
ACL 40ms sniff	Slave	1.5	mA
ACL 1.28s sniff	Slave	0.24	mA
SCO HV1	Slave	34	mA
SCO HV3	Slave	23	mA
SCO HV3 30ms sniff	Slave	17	mA
Parked 1.28s beacon	Slave	0.18	mA

FM Operation Mode	Connection Type	Average	Unit
FM receiver	-	18	mA

Chip Operation Mode	Connection Type	Average	Unit
Standby with host connection	-	30	µA
Reset (active low)	-	42	µA

(a) Bluetooth measurements made with FM disabled.
(b) All measurements made at UART rate 115.2kbps.

Typical Peak Current @ +20°C[a]	
Device Activity/State	**Current (mA)**
Peak current during cold boot	57.9
Peak TX current master	51.5
Peak RX current master	39.0
Peak TX current slave	52.0
Peak RX current slave	45.5
Conditions	
Temperature	20°C
Firmware	HCI 22 (provisionally)
VREGIN, VDD_PIO, VDD_PADS	1.8V
Host interfaces	UART, I^2C
UART baud rate	115200
Clock source	26MHz external
Output power	0dBm
FM input signal level	-47dBm
FM frequency level	98.1MHz

(a) Bluetooth mode only. Bluetooth measurements made with FM mode disabled.

13 CSR Bluetooth Software Stacks

BlueCore5-FM WLCSP is supplied with Bluetooth v2.1 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.

13.1 BlueCore HCI Stack

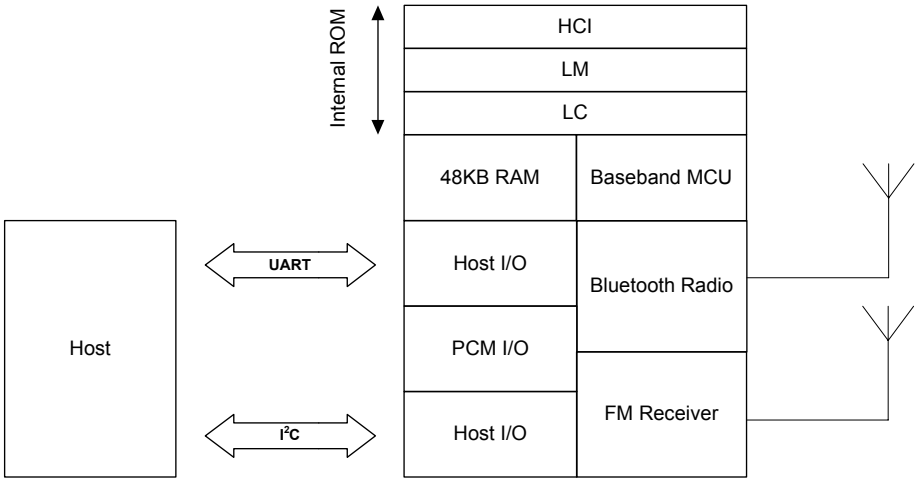


Figure 13.1: BlueCore HCI Stack

In the implementation shown in Figure 13.1 the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers including the application.

13.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

CSR supports the following Bluetooth v2.1 + EDR functionality:

- Secure simple pairing
- Sniff subrating
- Encryption pause resume
- Packet boundary flags
- Encryption
- Extended inquiry response

Bluetooth v2.0 + EDR mandatory functionality:

- Adaptive frequency hopping (AFH), including classifier
- Faster connection - enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

Optional Bluetooth v2.0 + EDR functionality supported:

- Adaptive Frequency Hopping (AFH) as Master and Automatic Channel Classification
- Fast Connect - Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- Extended SCO (eSCO), eV3 +CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.1 + EDR specification:

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard USB v1.1 and UART HCI Transport Layers
- All standard Bluetooth radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps (this is the maximum allowed by Bluetooth v2.1 + EDR specification)
- Operation with up to seven active slaves
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7 (BlueCore5-FM WLCSP supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.1 + EDR specification)
- Maximum number of simultaneous active SCO connections: 3
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from www.csr.com.

13.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP), a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Supports H4DS, a proprietary alternative to the standard Bluetooth UART Host Transport, supporting Deep Sleep for low-power applications
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BlueCore Command (BCCMD), provides:
  - Access to the chip's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Bluetooth radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor
- A block of BCCMD commands provides access to the chip's Persistent Store configuration database (PS). The database sets the device's Bluetooth address, Class of Device, Bluetooth radio (transmit class) configuration, SCO routing, LM, USB constants, etc.
- A UART break condition can be used in three ways:
  1. Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  2. Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  3. With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a Deep Sleep state.)
- A block of Bluetooth radio test or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Hardware low power modes: Shallow Sleep and Deep Sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the chip's PCM ports (at the same time as routing any remaining SCO channels over HCI).

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

13.2 CSR Development Systems

CSR's BlueLab Multimedia and Casira development kits are available to allow the evaluation of the BlueCore5-FM WLCSP hardware and software, and as toolkits for developing on-chip and host software.

14 Ordering Information

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	67-ball WLCSP	4.12 x 4.04 x 0.66mm (max.) 0.4mm pitch	Tape and reel	BC51E129AXX-IYH-E4[a]

[a] Until BlueCore5-FM WLCSP reaches **Production,** status order number is BC51E129AXX-ES-IYH-E4.

Minimum Order Quantity

2kpcs taped and reeled

XX = Firmware revision

To contact a CSR representative, send e-mail to sales@csr.com or go to www.csr.com/contacts.htm.

14.1 Tape and Reel Dimensions

The tape and reel are in accordance with EIA-481-2. For information on tape and reel packing and labelling see *IC Packing and Labelling Specification*.

14.1.1 Tape Orientation and Dimensions

The general orientation of the BGA in the tape is as shown in Figure 14.1.

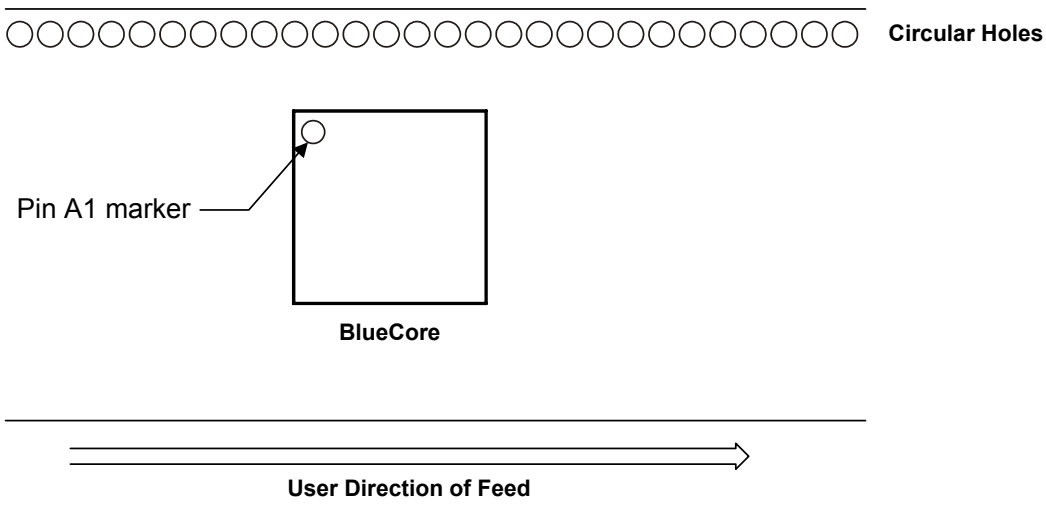


Figure 14.1: Tape and Reel Orientation

14.1.2 Reel Information

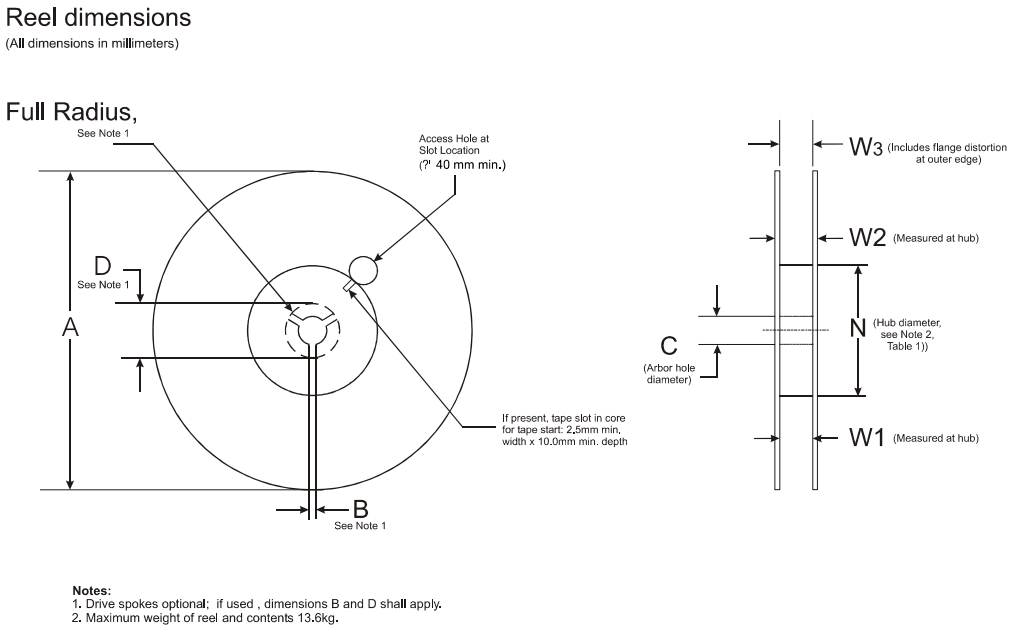


Figure 14.2: Reel Dimensions

Package Type	Tape Width	A Max	B	C	D Min	N Min	W1	W2 Max	W3		Units
									Min	Max	
6 x 6mm VFBGA	16	332	1.5	13.0 (+0.5/-0.2)	20.2	50	16.4 (+2.0/-0.0)	22.4	16.4	19.1	mm

Table 14.1: Reel Dimensions

14.2 Moisture Sensitivity Level (MSL)

15 Document References

Document	Reference, Date
Specification of the Bluetooth System	v2.1 + EDR, 26 July 2007
BlueCore5-FM FM API	CS-101761-SP (bcore -sp-021Pe), August 2006
Bluetooth and IEEE 802.11b/g Co-existence Solutions Overview	CS-101409-ANP (bcore-an-066P)
BCCMD Commands	CS-101482-SPP (bcore-sp-005P)
HQ Commands	CS-101677-SPP (bcore-sp-003P)
Typical Solder Reflow Profile for Lead-free Devices	CS-116434-ANP
IC Packing and Labelling Specification	CS-112584-SPP

16 Terms and Definitions

Term	Definition
3G	3rd Generation of Multimedia
8DPSK	8 phase Differential Phase Shift Keying
π/4 DQPSK	pi/4 rotated Differential Quaternary Phase Shift Keying
ACL	Asynchronous Connection-Less. Bluetooth data packet
ADC	Analogue to Digital Converter
AFC	Automatic Frequency Control
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
A-law	Audio encoding standard
ALU	Arithmetic Logic Unit
AM	Amplitude Modulation
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BAF	Audio Frequency Band
balun	A device that connects a balanced line to an unbalanced line; for example, a twisted pair to a coaxial cable
BCCMD	BlueCore™ Command
BCSP	BlueCore Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BIST	Built-In Self-Test
BlueCore®	Group term for CSR's range of Bluetooth chips
Bluetooth™	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
BW	Band Width
CDMA	Code Division Multiple Access
C/I	Carrier-to-cochannel interference ratio
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CQDDR	Channel Quality Driven Data Rate
CRC	Cyclic Redundancy Check
CS	Channel Separation
CS#	Chip Select (Active Low)
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter

Term	Definition
dBm	Decibels relative to 1mW
DC	Direct Current
DDS	Direct Digital Synthesis
DEVM	Differential Error Vector Magnitude
DFU	Device Firmware Upgrade
DNL	Differential Non-Linearity
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quarternary Phase Shift Keying
DSP	Digital Signal Processor
EDR	Enhanced Data Rate
eSCO	extended SCO
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
FSK	Frequency Shift Keying
GCI	General Circuit Interface
GND	Ground
GSM	Global System for Mobile communications
H4	UART-based HCI transport, described in section H4 of v1.0b of Bluetooth Specification
H4DS	H4 Deep Sleep
HCI	Host Controller Interface
HQ	Host Query
IC	Integrated Circuit
I^2C	Inter-Integrated Circuit
I^2S	Inter-Integrated Circuit System
IF	Intermediate Frequency
IIR	Infinite Impulse Response
INL	Integral Non-Linearity
I/O	Input/Output
IQ Modulation	In-Phase and Quadrature Modulation
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
JEDEC	Joint Electron Device Engineering Councils
ksps	KiloSamples Per Second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LJ	Left Justified
LM	Link Manager

Term	Definition
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LSB	Least-Significant Bit
µ-law	Audio Encoding Standard
Mbps	Mega bits per second
MCU	MicroController Unit
MMU	Memory Management Unit
MISO	Master In Serial Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
OHCI	Open Host Controller Interface
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PD	Pull-Down
PDA	Personal Digital Assistant
PICS	Protocol Implementation Confirmation Statement or Profile Implementation Confirmation Statement (both are used)
PIO	Parallel Input Output
Pk-Pk	Peak-to-Peak
PLL	Phase Lock Loop
ppm	parts per million
PS	Persistent Store
PS Key	Persistent Store Key
PSRR	Power Supply Rejection Ratio
PSU	Power Supply Unit
PU	Pull-Up
RAM	Random Access Memory
RDS	Radio Data System
RE#	Read enable (Active Low)
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RJ	Right Justified
RL	Load Resistance
rms	root mean squared

Term	Definition
RoHS	The Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read-Only Memory
RS232	Recommended Standard 232. A TIA/EIA standard for serial transmission between computers and peripheral devices (modem, mouse, etc.)
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SD	Secure Digital
SDK	Software Development Kit
SDP	Service Discovery Protocol
SNR	Signal Noise Ratio
SPI	Serial Peripheral Interface
TBA	To Be Announced
TBD	To Be Defined
TCXO	Temperature Controlled crystal Oscillator
TFBGA	Thin Fine-Pitch Ball Grid Array
THD	Total Harmonic Distortion
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UHCI	Upper Host Control Interface
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
W-CDMA	Wideband Code Division Multiple Access
WCS	Wireless Co-existence System
WE#	Write Enable (Active Low)
WLCSP	Wafer-Level Chip Scale Package
XAP	Low-power silicon-efficient RISC microprocessor
XTAL	Crystal

17 Document History

Revision	Date	History
bc05-ds-006Pa	04 APR 06	Original publication of this document
bc05-ds-006Pb	24 MAY 06	Pinout confirmed and application schematic updated
CS-110333-DSP3 (bc05-ds-006Pc)	06 OCT 06	Corrected pinout information
4	12 OCT 06	Updated application schematic
5	18 OCT 06	Corrected package dimension
6	27 SEP 07	Updates for Bluetooth v2.1 + EDR. Clarification on Sleep Clock description and SLEEP_CLK. PCB, solder reflow, and tape and reel information added. RF characterisation moved into Performance Specification. Editorial changes.
7	28 SEP 07	Corrections to pin numbers in Package Information section
8	08 OCT 07	Corrected Device Terminal Functions